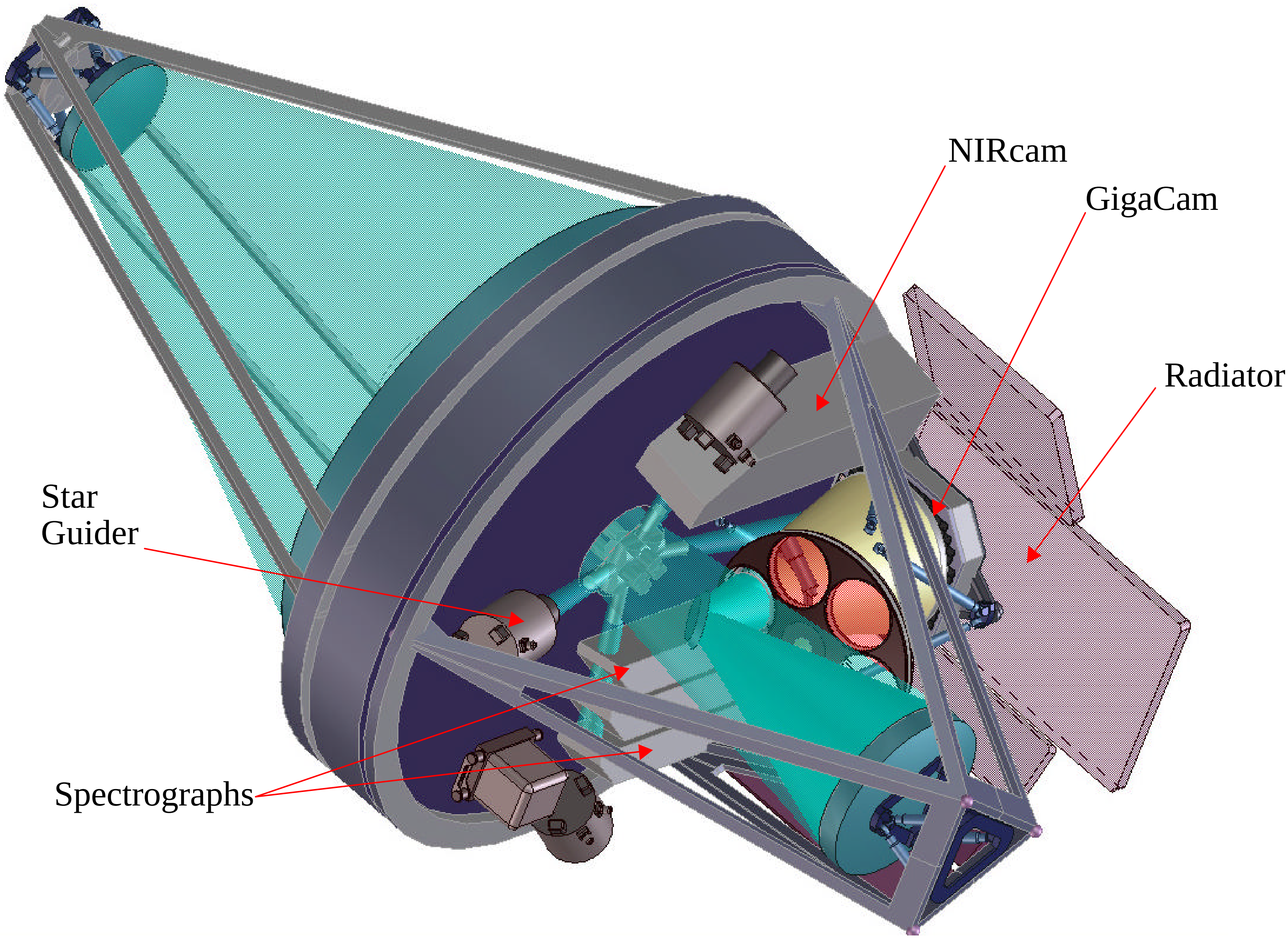
Overview of Instrument Talks

Optical imager — GigaCam	Chris Bebek
Electronics architecture	Henrik von der Lippe
ASIC development	Gerard Smadja
NIR imager — NIRcam/WNIRcam	Greg Tarlé
Spectrographs	Eric Prieto
HgCdTe technology for SNAP	James Graham
CCD technology	Steve Holland (Friday)

SNAP “Baseline”



Instrument Deployment

In the baseline design, the instruments each have their own light pick-off and focal plane.

This raises three concerns:

1. Establishing and keeping the instruments in focus simultaneously.
2. Establishing strong coupling between the precision star guiders and the focal planes.
3. A second complex light path has to be created if we want an IR imager larger than 1’ x 1’.

A concept in early development is to coalesce the instruments around the main focal plane, **FIDO**, fully integrated focal plane option.

Issues associated with FIDO:

- Differing plate scales of CCDs and IR detectors due to different pixel sizes.
- Potentially different operating temperatures for CCDs and IR detectors.
- Implementation of shutter and filters.

Decision will be made in June-July 2001.

FIDO Example

Components:
- **236 CCDs**
- **24 1k x 1k HgCdTe**
- **2 spectrographs**
- **8 star guider CCDs**

IR:

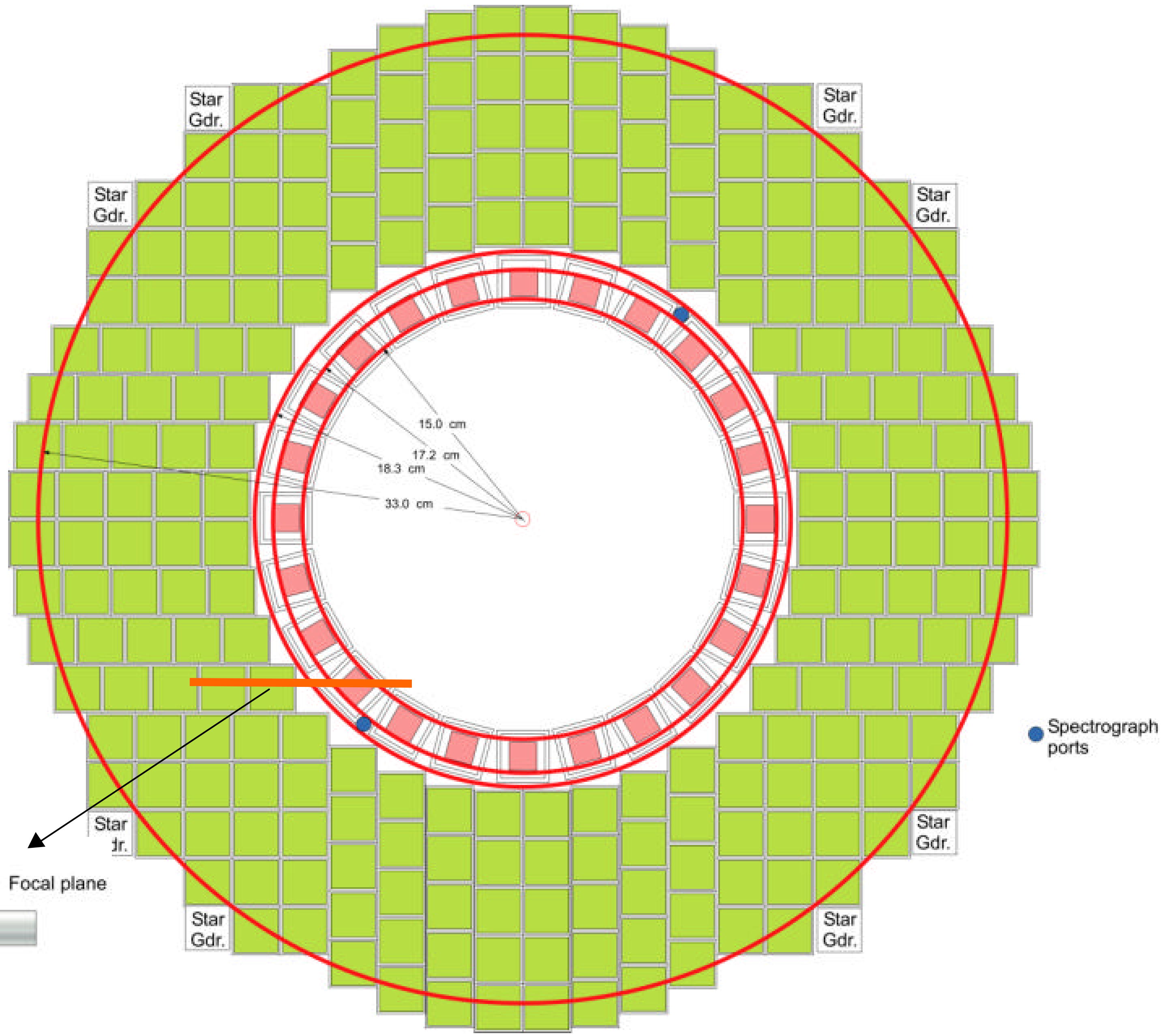
0.028 sq. deg.

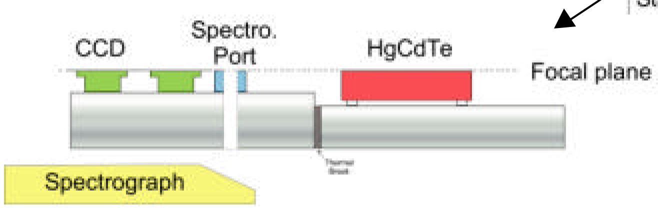
0.125 asec/pixel

Visible:

0.87 sq. deg.

0.07 asec/pixel





GigaCam
An Optical Imager for SNAP

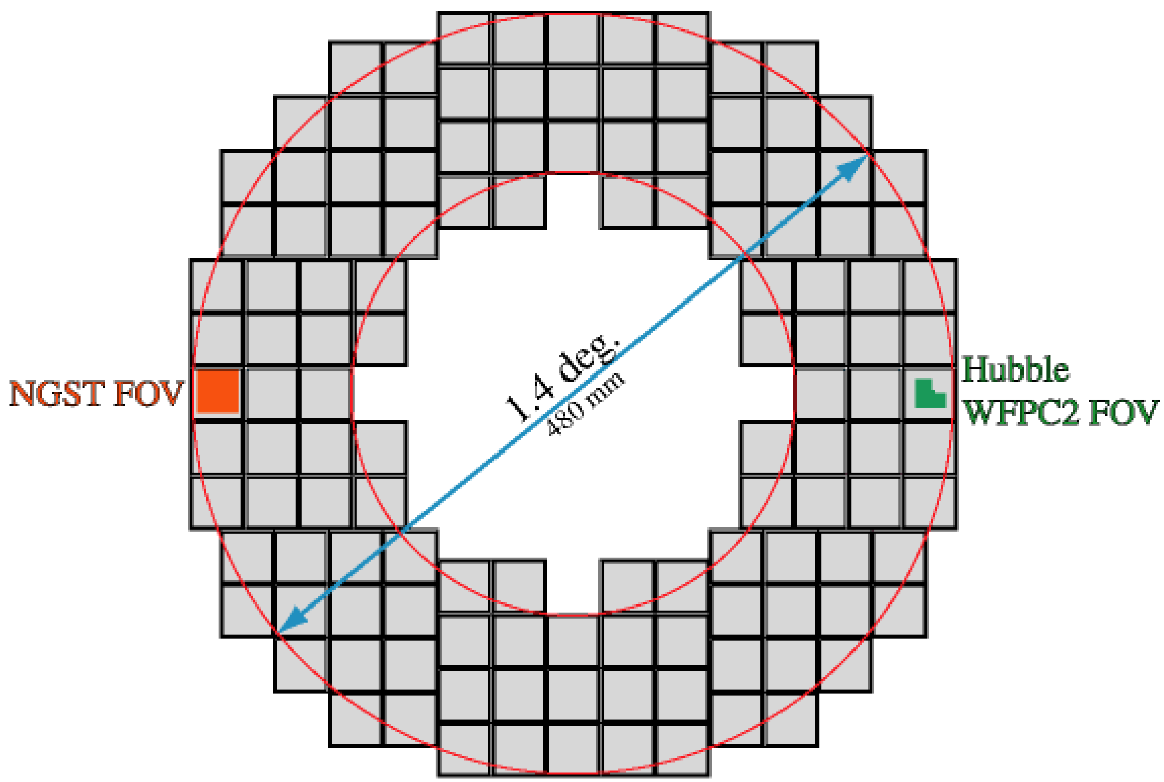
Chris Bebek

Cornell University/LBNL

Overview

Talk overview

- **Development and commercialization of a new CCD.**
- **Gearing up to demonstrate that the CCDs are scientific grade devices.**
- **Our plan to understand the CCDs performance in a space.**
- **Development of packaging technology to allow a large mosaic.**
- **Development of radiation shielding concept.**



Science driven requirements

Populate 1° x 1° focal plane with small dead space.

Broad spectral response with high quantum efficiency.

Low read noise to allow stacking multiple exposures.

Low dark current to support long exposures.

Stable performance in presence of radiation (>3 yrs).

Field-of-view	Approximately 1° x 1°
Plate Scale	0.07 to 0.10 arcsec/pixel (0.10 nominal)
Pixelization	Approx. 32k x 32k CCD mosaic
Wavelength coverage	350 nm – 1000 nm
Detector Type	High-Resistivity p-channel CCDs
Detector Architecture	2.5k x 2.5k, 12 or 10.5 μm pixel
Detector Array Temperature	135 - 150 K
Detector Quantum Efficiency:	65% @ 1000 nm, 92% @ 900 nm, >85% @ 400-800 nm
Photometric Accuracy	1% relative
Read Noise	4 e- @100 kHz
Exposure Time	100 sec to 1000 sec (single exposures)
Dark Current	0.04 e-/sec/pixel
Readout Time	20 sec

R&D issues

Main R&D issues

- Develop and commercialize a new type of CCD.
- Packaging the CCDs that allows efficient tiling of a focal plane.
- Protecting the CCDs from thermal and particle backgrounds.

Technical challenges

- Producing 300 μm thick, 150 mm wafers at a commercial foundry.
- Testing large numbers of devices.

Why Develop a New CCD?

We believe we can uniquely achieve the following attributes:

Populate 1° x 1° focal plane with small dead space,
88% packing efficiency.

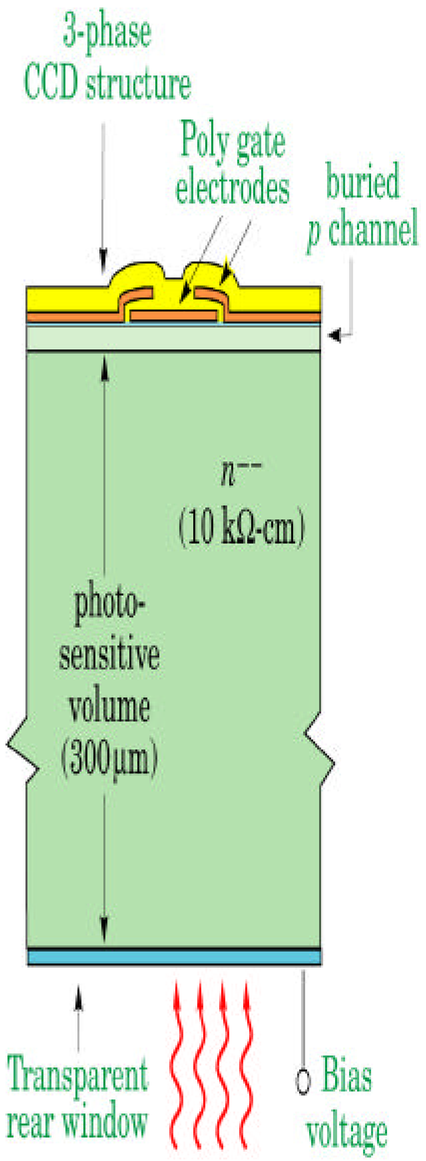
Broad spectral response with high quantum efficiency,
High QE from 350 nm to 1000 nm.

Low read noise to allow stacking multiple exposures,
$2e^-$ at 100 kHz read rate.

Low dark current to support long exposures,
0.001 e^-/s.

Stable performance in presence of radiation (>3 years).
Radiation tolerant charge transfer, dark current, and read noise.

New CCD Technology



Advantages:

1) Conventional MOS processes with no thinning => "inexpensive"
2) Full quantum efficiency to > 1 μm => no fringing
3) Good blue response with suitably designed rear contact
4) Radiation tolerant

Disadvantages:

1) Enhanced sensitivity to radiation (x-rays, cosmic rays, radioactive decay)

- **New kind of CCD developed at UCB/LBNL.**
- **High resistivity, *n*-type, *p*-channel, fully depleted silicon – same as used in HEP silicon vertex detectors.**
- **Rear illuminated.**
- **Antireflection coating.**
- **Thin polysilicon window for good blue response.**
- **Good QE at 1 μm and no fringing – 300 μm thickness and λ_{abs} ~100 μm.**
- **No costly thinning of devices.**
- **High-purity silicon has better radiation tolerance for space applications.**

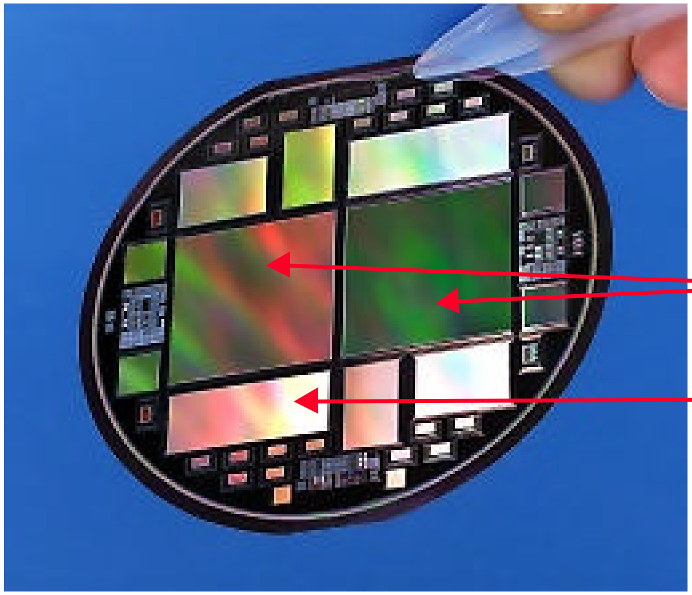
Steve Holland will talk more on the technology Friday afternoon.

Issues for CCDs

- Charge transfer efficiency
  - Charge dependence
  - T dependence
  - Radiation damage
- Read noise
  - Readout rate
  - Radiation damage
- Defects
- Erasure
- Cross talk

- Clock shaping
- Diffusion
- Pixel size
  - Well depth
  - Intra-pixel response
- Yield
  - Grinding/polishing
  - Quality
- Precision assemblies
- Shielding

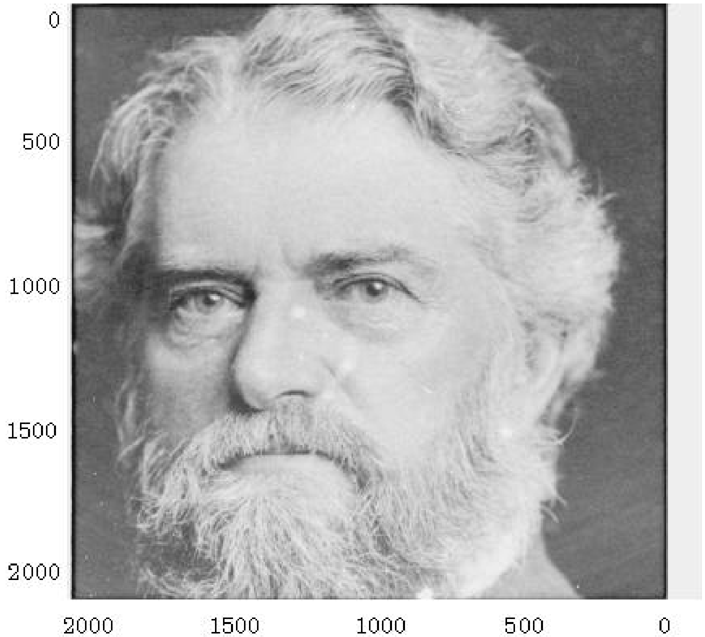
LBNL 2k x 2k

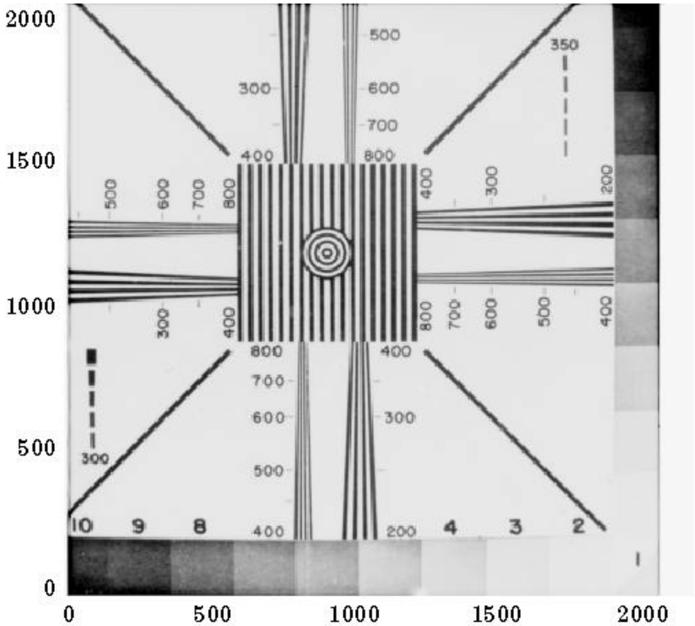


First large format CCD made at LBNL

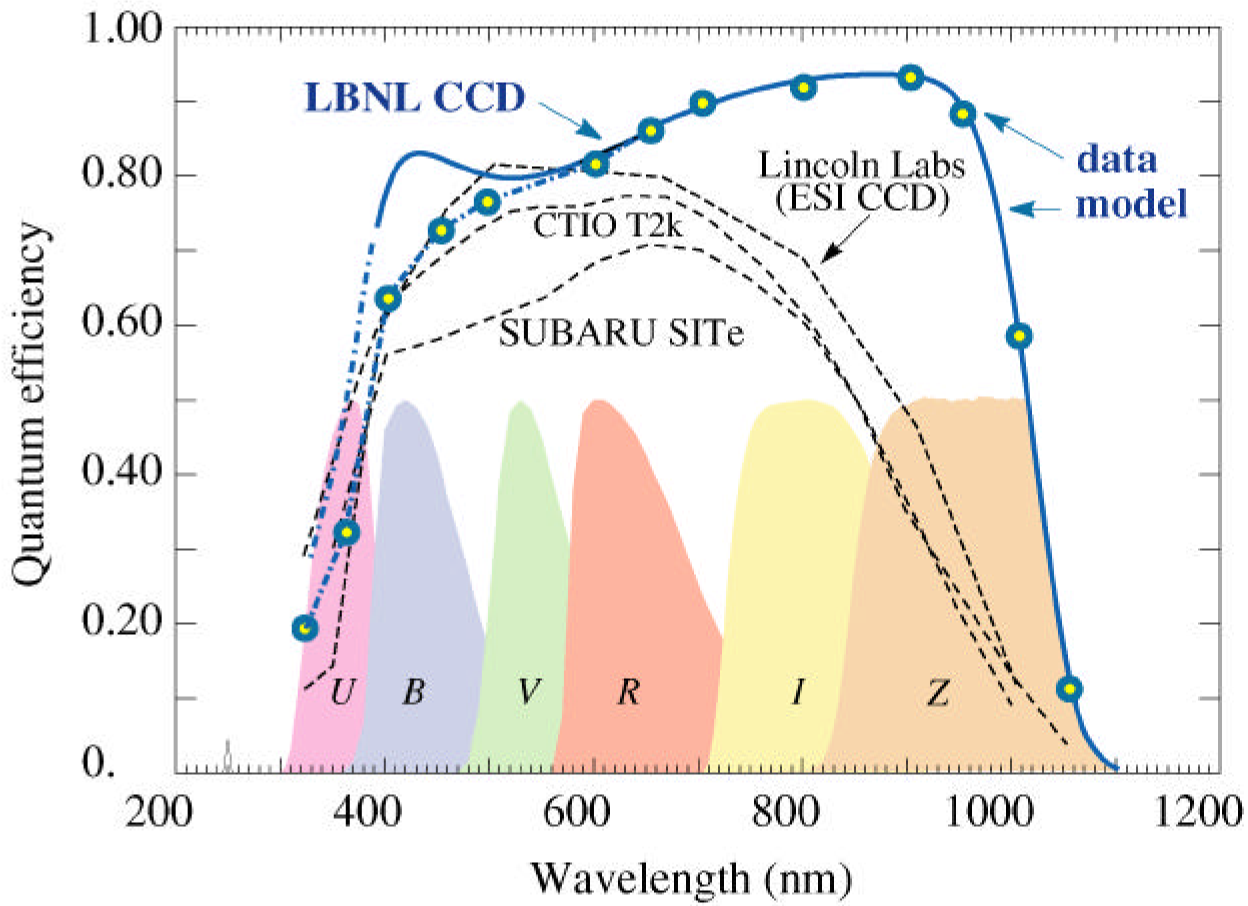
2k x 2k, 15 μm pixels.

1980 x 800, 15 μm pixels.





LBNL 2k x 2k results



Quantum efficiency

Note uniquely high QE from 0.7 mm to 1 mm.

Measurements courtesy of Lick/UCSC.

LBNL 2k x 2k results

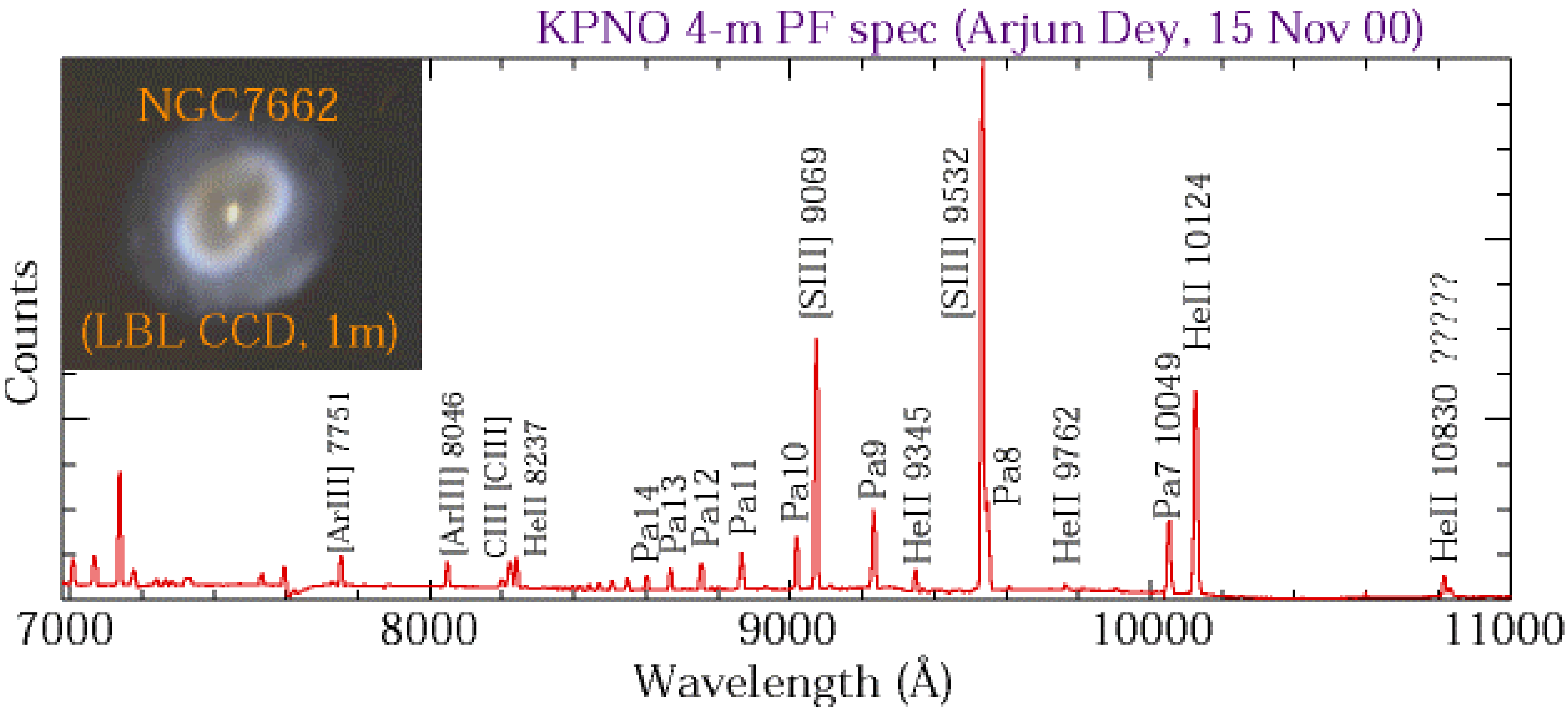
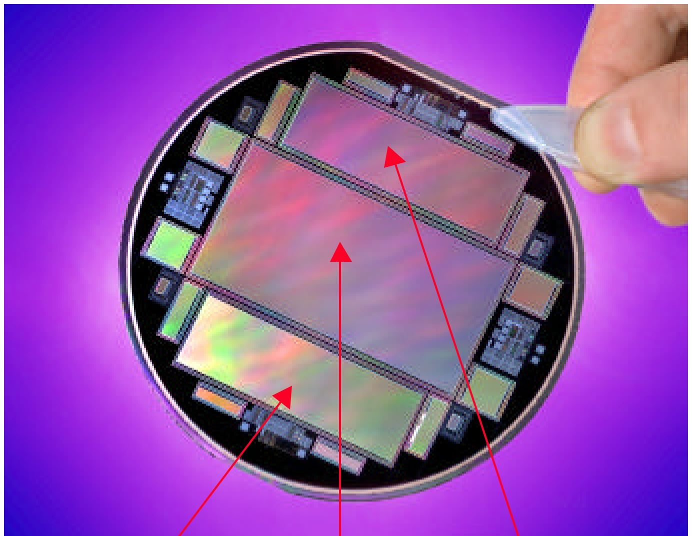


Image: 200 x 200 15 mm LBNL CCD in Lick Nickel 1m.
Spectrum: 800 x 1980 15 mm LBNL CCD in NOAO KPNO spectrograph.

LBNL 2k x 4k



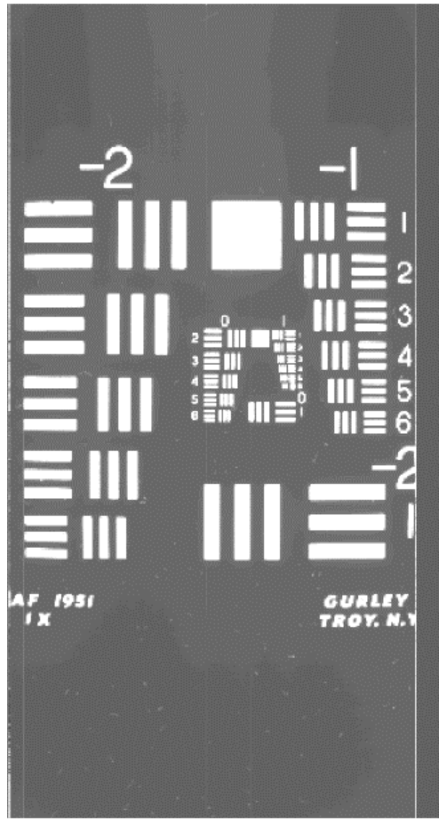
1478 x 4784
10.5 μm

2k x 4k
15 μm

1294 x 4186
12 μm

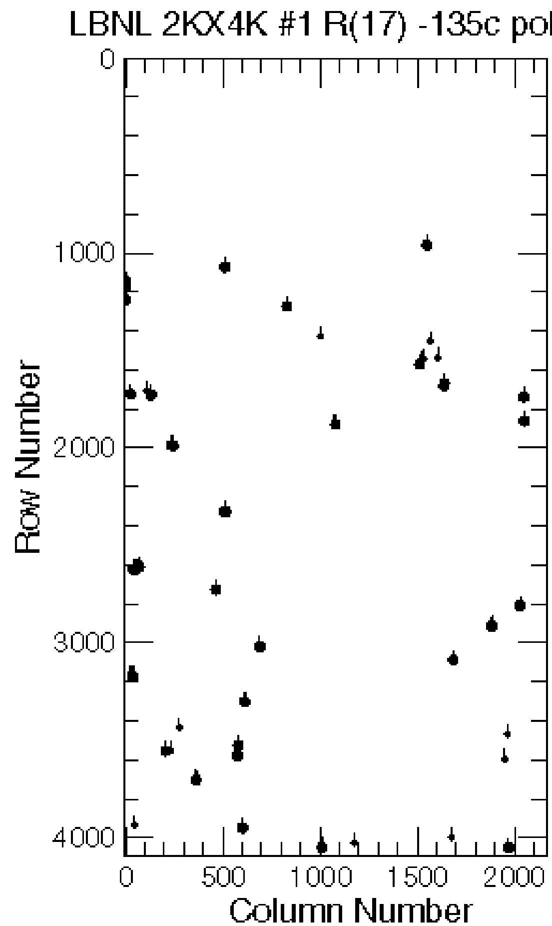
USAF test pattern.

LBNL 2KX4K #1 R(17) -135c image



Size: 512 Rows, 272 Cols Origin (0,0)

Trap sites found by pocket pumping.



Measurements courtesy of Lick/UCSC.

Next LBNL CCDs

In February, the Micro Systems Lab will start production of wafers concentrating on 2k x 4k 15 μm devices.

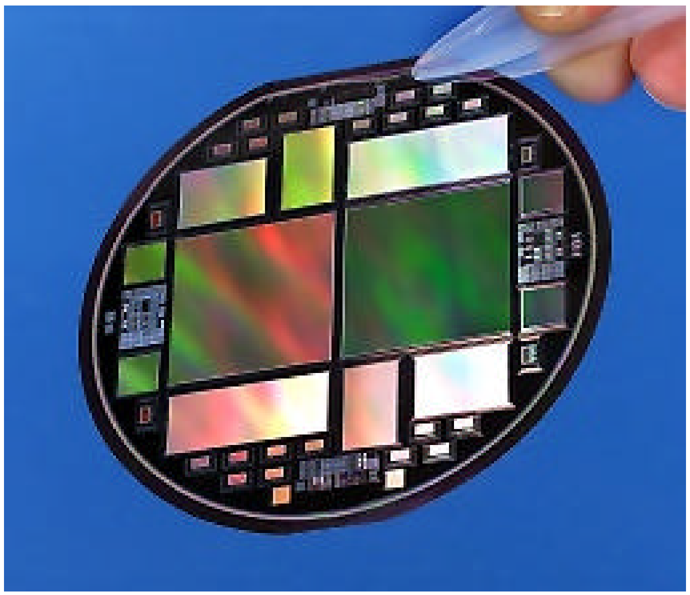
There will be no SNAP specific devices on the wafers.

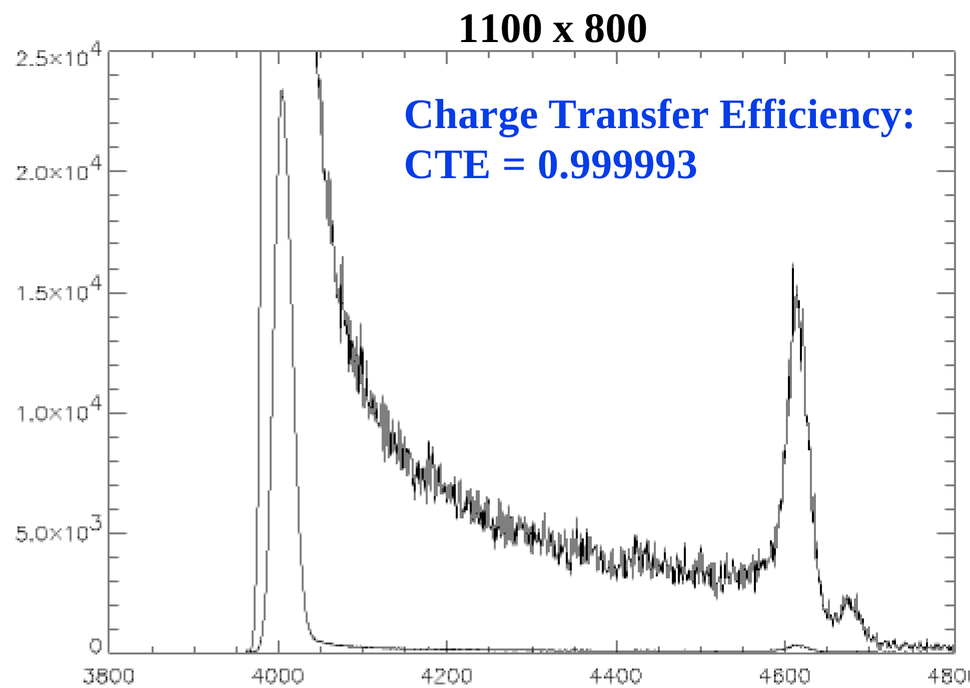
Rather, we will use the yields of this run to understand MSL's role as a backup foundry for SNAP.

Four SNAP-sized CCDs can be fit on a dedicated 100 mm wafer.

Commercial 2k x 2k

The LBNL 2k x 2k layout and recipe where transferred to a commercial foundry.





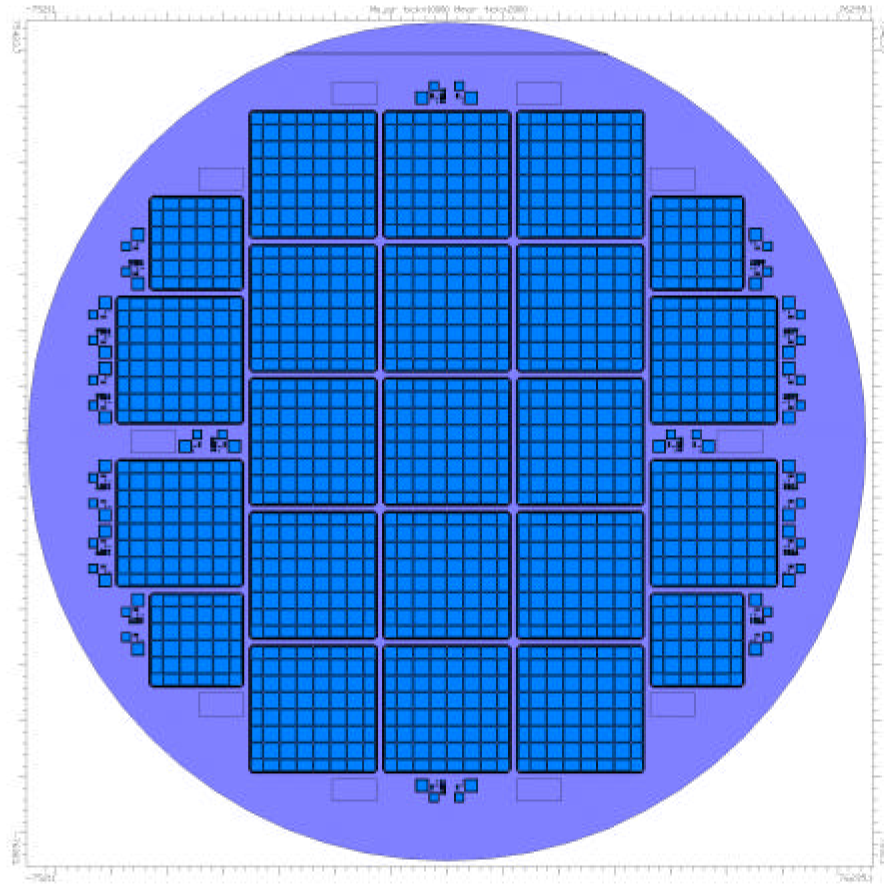
^{55}Fe spectrum

Commercial PIN Diodes

Array of 3 mm x 3 mm PIN diodes on a 150 mm diameter wafer.
Due January 2001.

First use of 300 μm 150 mm wafer by the vendor – usually 600 μm.

This will be wafer probed to make an *x-y* dark current to look for any variations in processing.



Commercial SNAP CCD

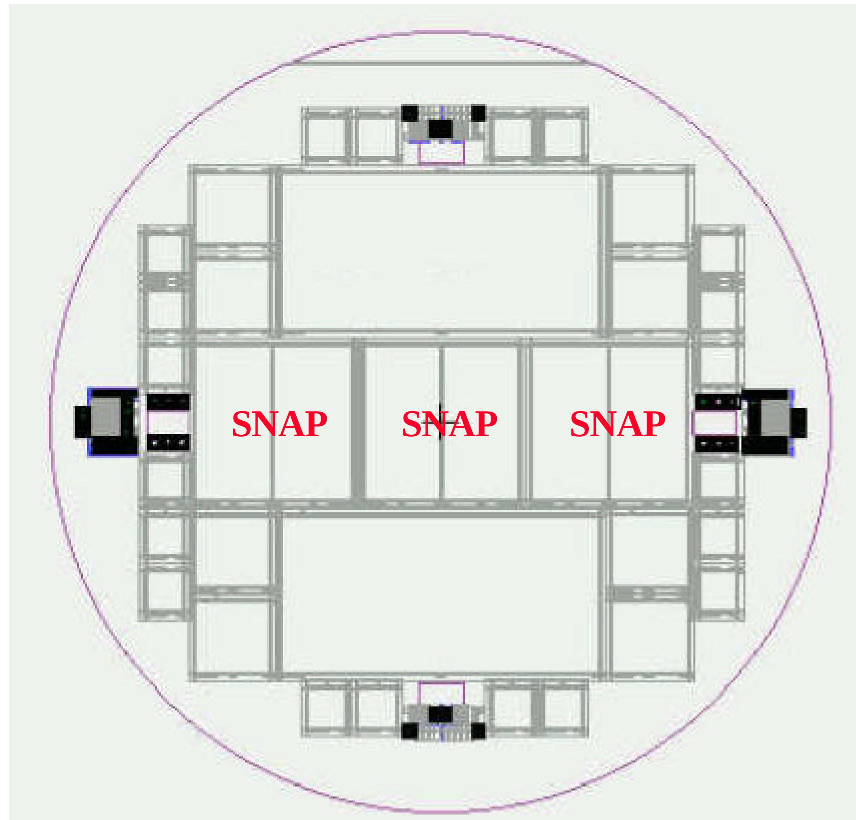
January submission.
 Lot 1 - 150 mm, 600 μm thick.
 Lot 2 - 150 mm, 300 μm thick.

Will contain SNAP CCDs
 2.5k x 2.5k 12 μm w/ vertical notch.
 2.5k x 2.5k 12 μm w/o vertical notch.
 2.8k x 2.8k 10.5 μm.

Will see if vendor can meet 7 week delivery for lot 1 and 16 weeks for lot 2.

CCD size is chosen to fit within vendor's reticles, minimize charge transfer length, yet take advantage of large format to reduce parts count. The size also populates an LBNL 4" wafer efficiently.

A dedicated SNAP run can have 9 devices per wafer.



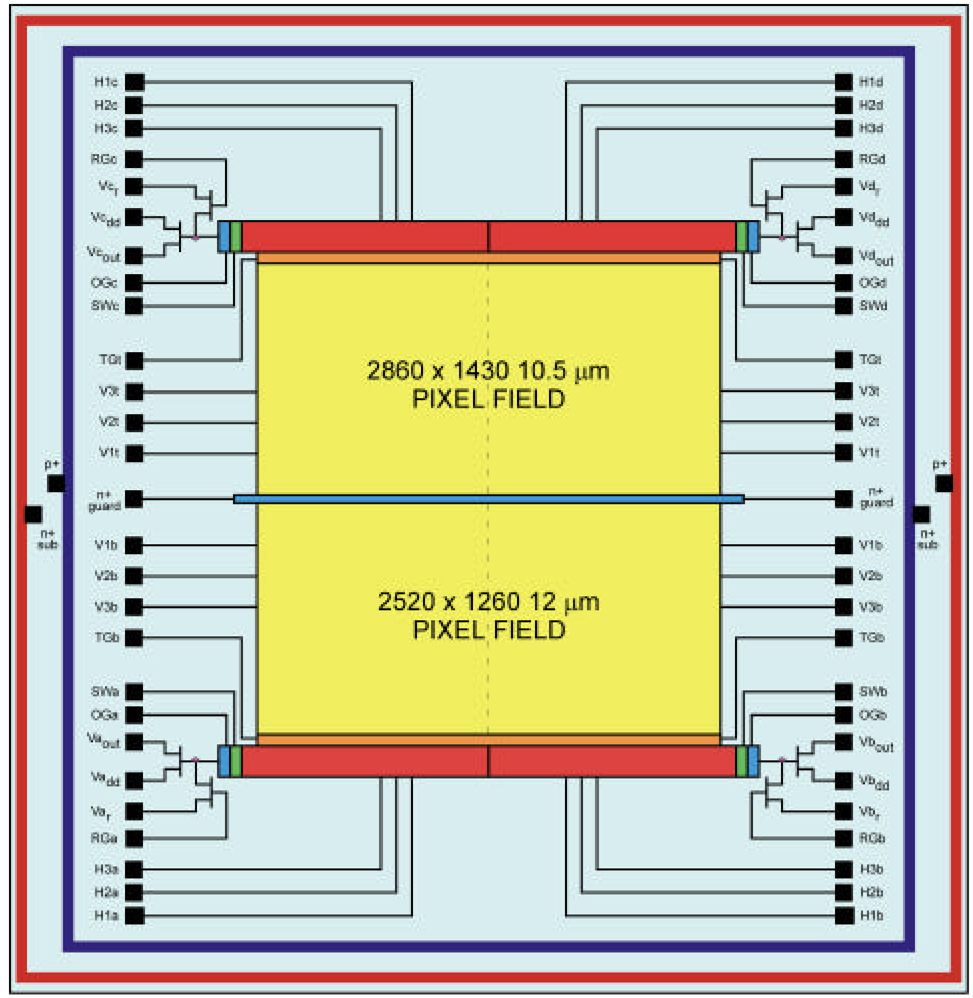
SNAP CCD Concept

2 x 2860 x 1430 10.5 mm
or
2 x 2520 x 1260 12.0 mm

4-corner and 2-corner readout.

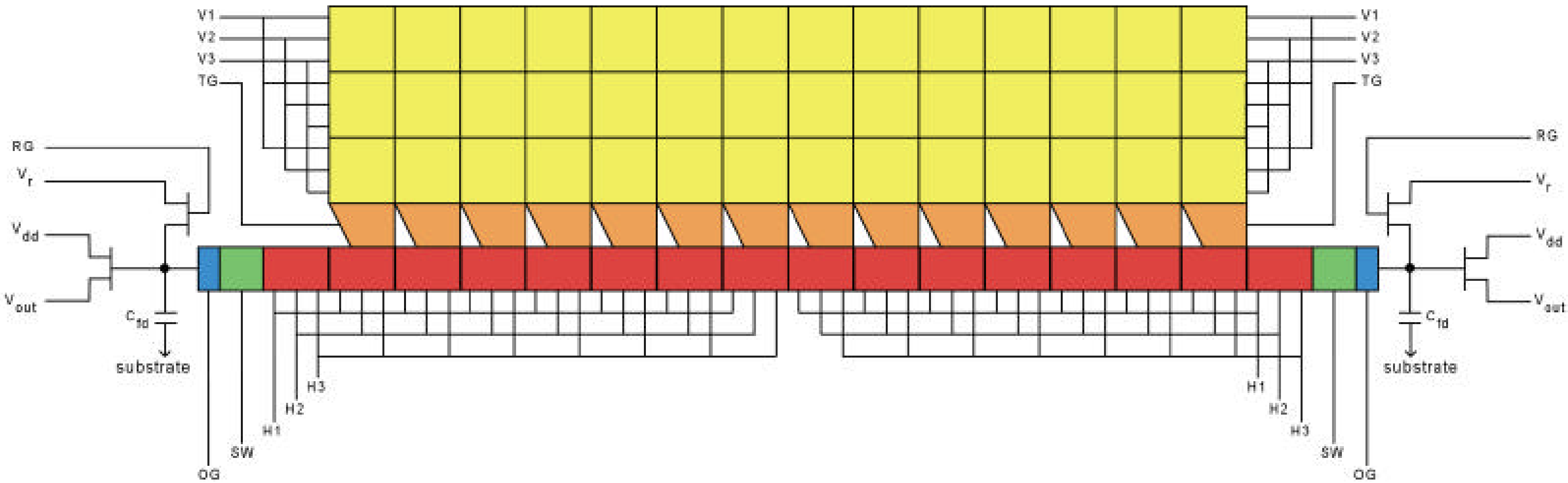
Read noise as low as 2 e.
Sensitivity as high as 6 mV/e.

Has top and bottom frame store (not shown).



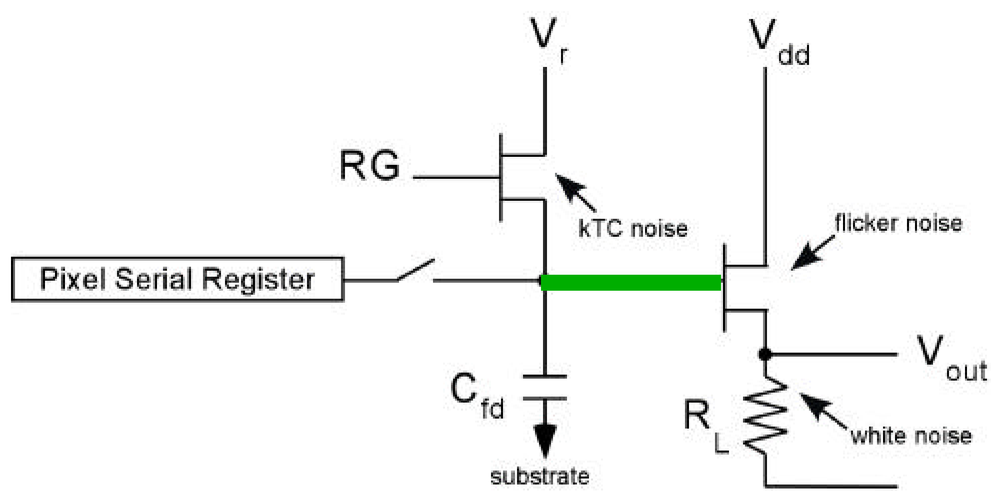
CCD Details

The figure is an abstraction of the serial register neighborhood.



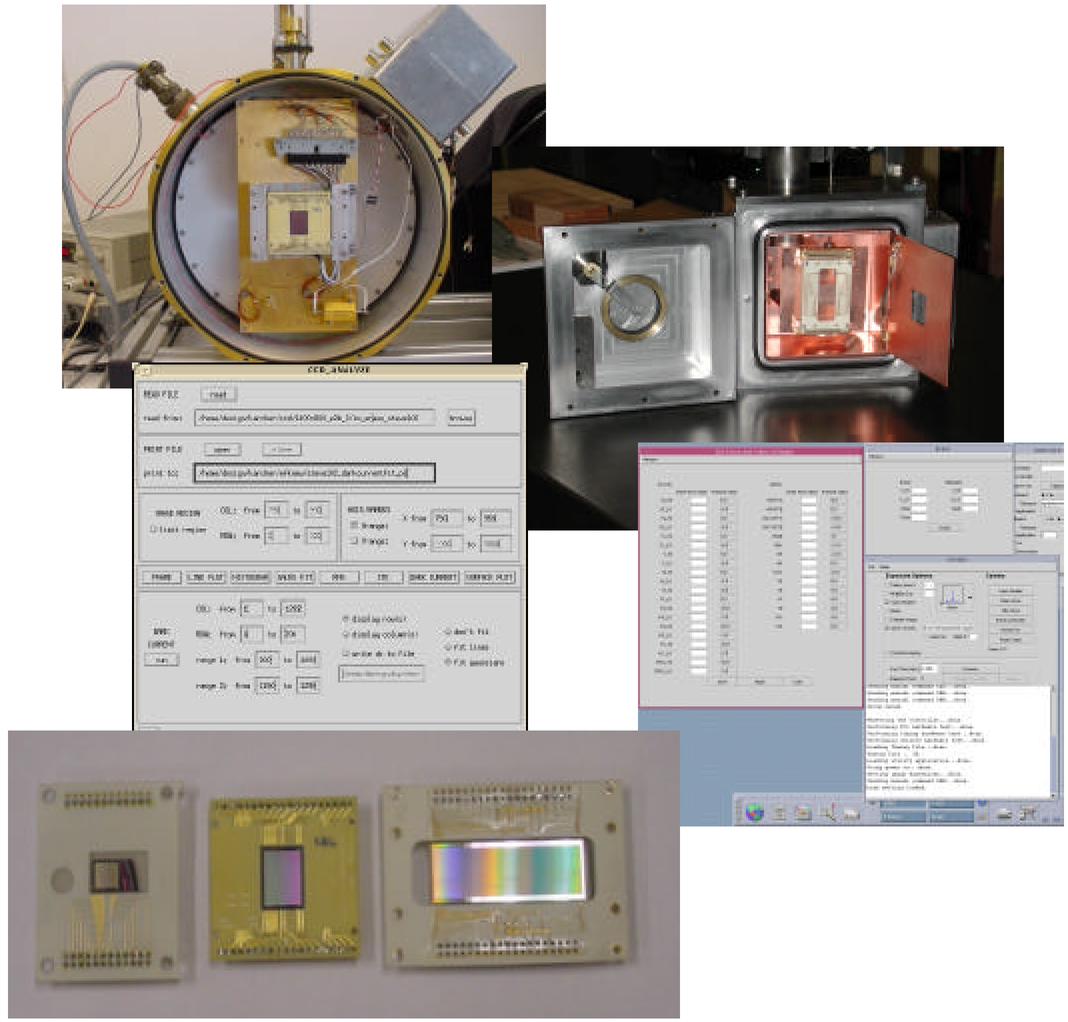
Define
- **Parallel**
- **Serial**
- **Read noise**

Remember the two transistors for later.



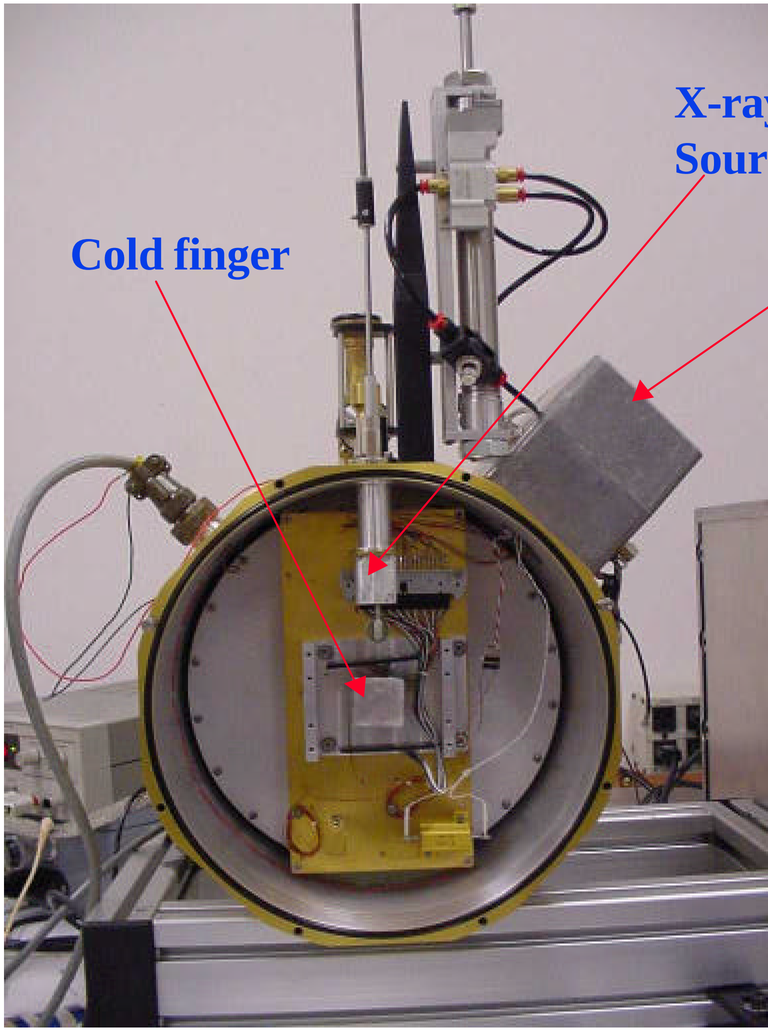
Test Facilities

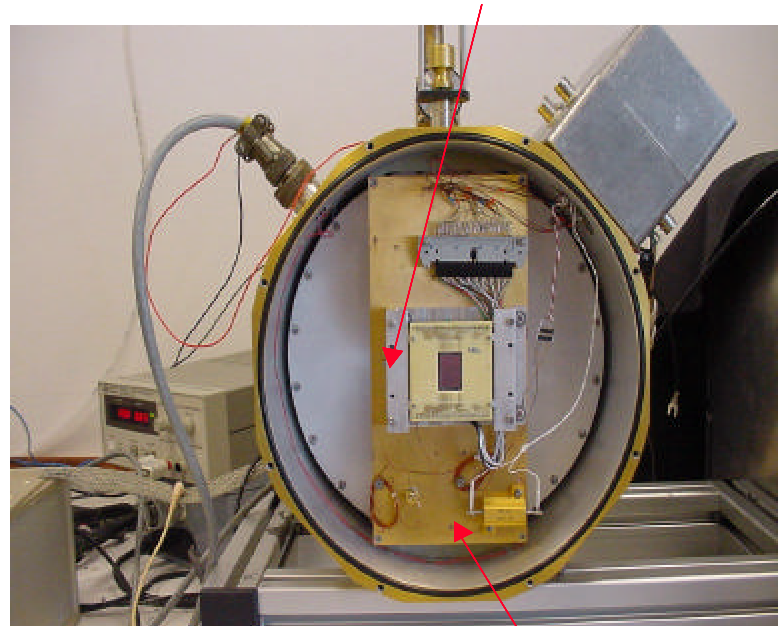
- 3 dewars
- 2 Leach readout controllers
- 2 SUN workstations
- PC with CD-RW
- Vacuum furnace
- -40C refrigerator
- Class 10000 clean room
- Wire-bonder



IR Labs Dewar

CCDs are operated at a nominal 150 K to make dark current small.
We use LN_2, a thermal switch, and a cold finger pressing against a face of the CCD (typically mounted on an AlN wafer).





Rapid Cycle Dewar

Chicken feeder dewar — ancient LBNL technology.

Quick release access plates, small volume and mass should give a cool-down/warm-up cycle under 2 hours.

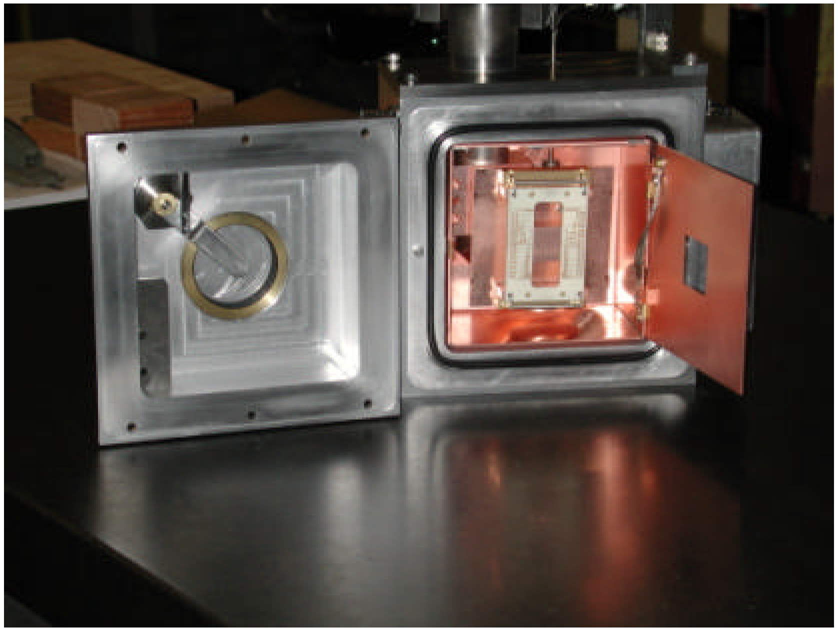


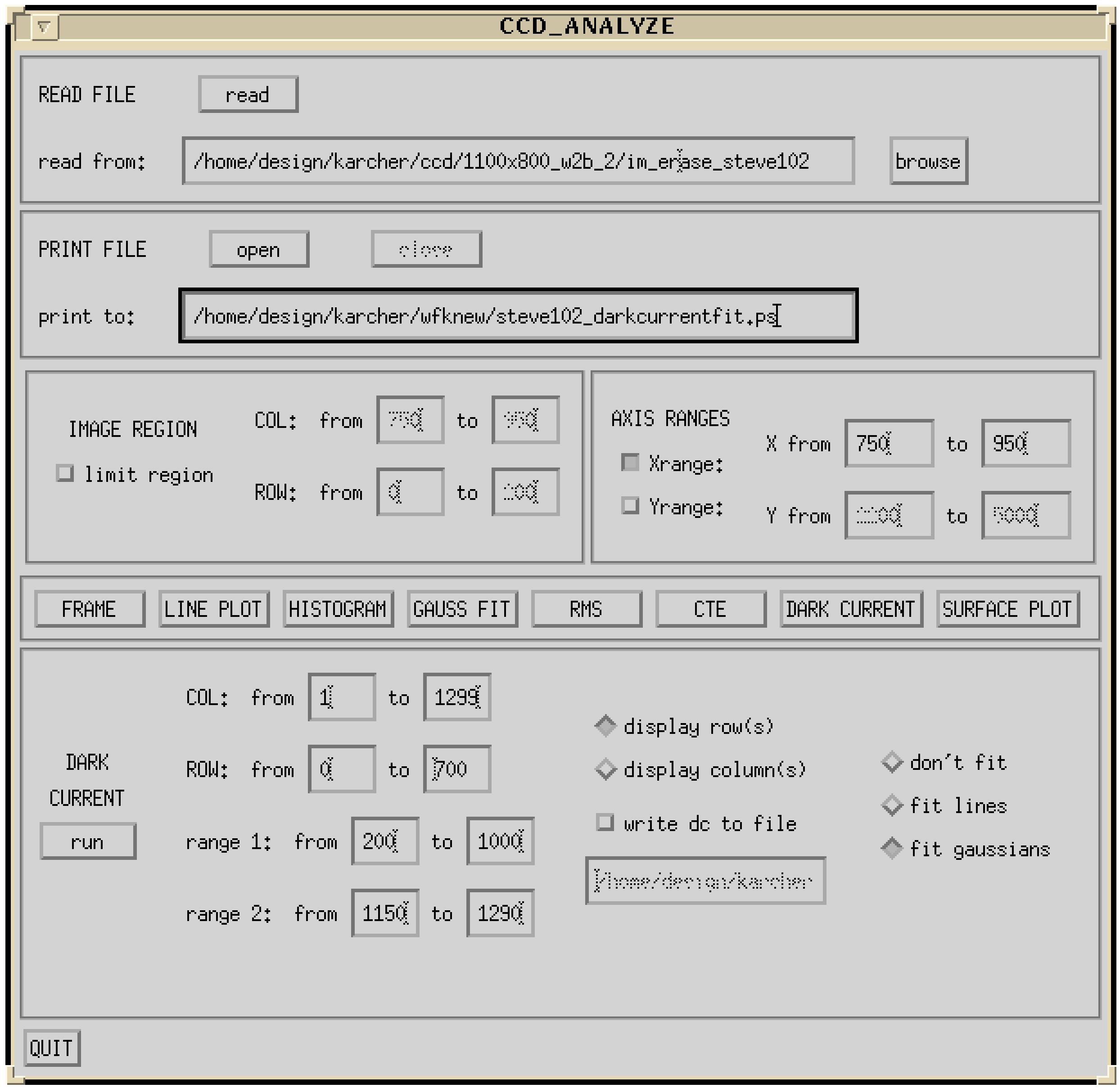
Image Analysis Software

IDL program started last summer by a student.

Easily extended to automate newly developed analysis routines or data views.

Analysis tool.

Dynamic window associated with analysis mode.

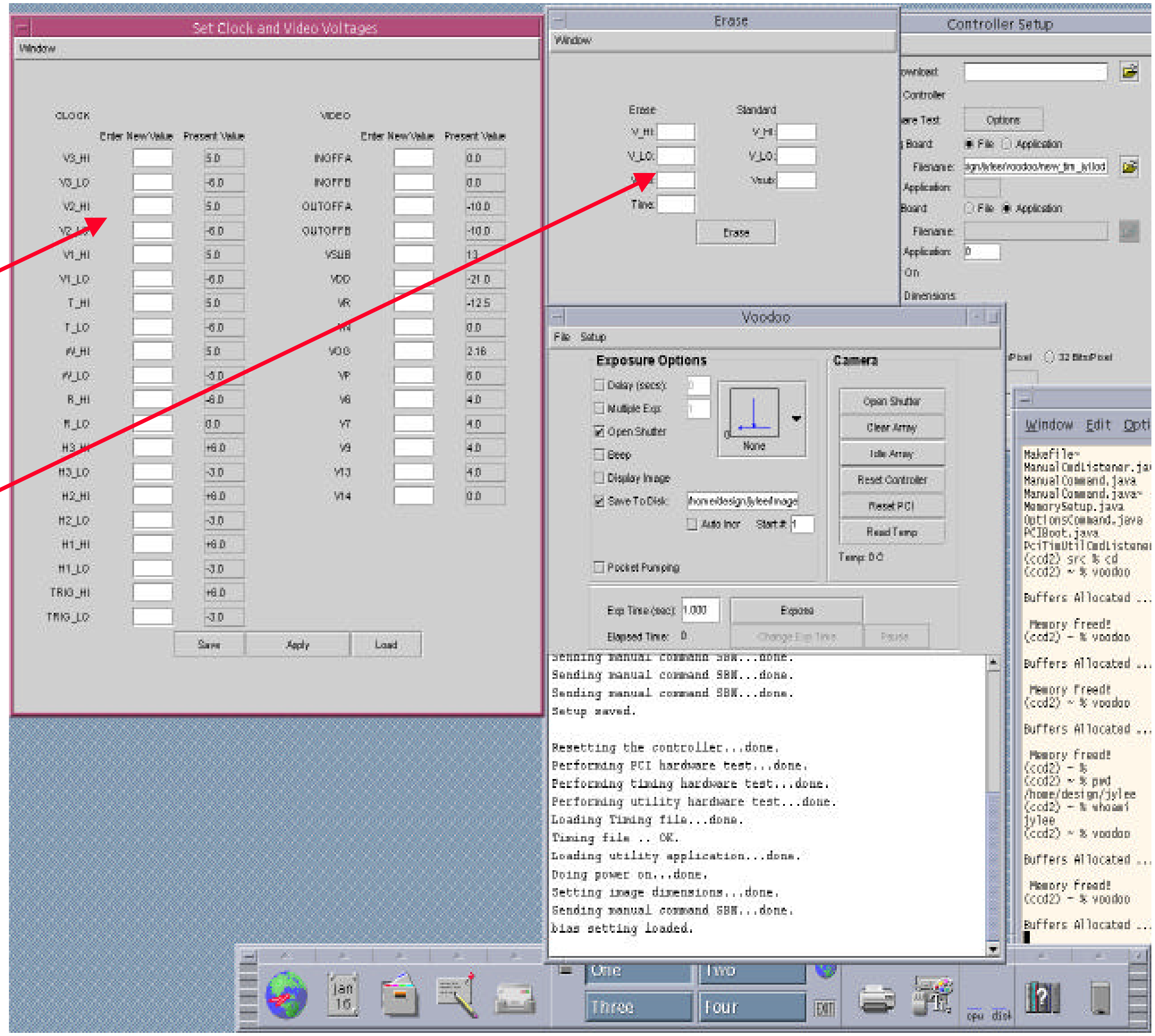


JAVA Controller Software

Adding functionality to the Voodoo JAVA interface.

Interactive modification of clock and bias voltages without reboots (required DSP code mods).

Add ability to gracefully enter and exit erase mode (required DSP code mods).

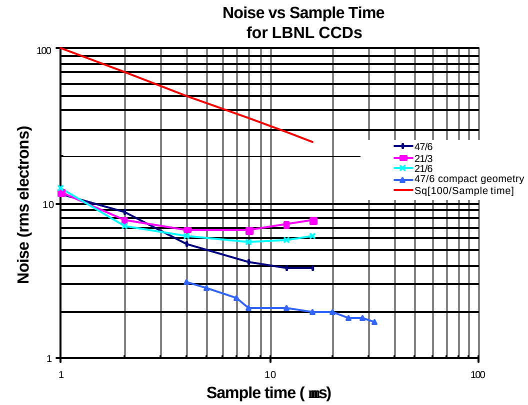


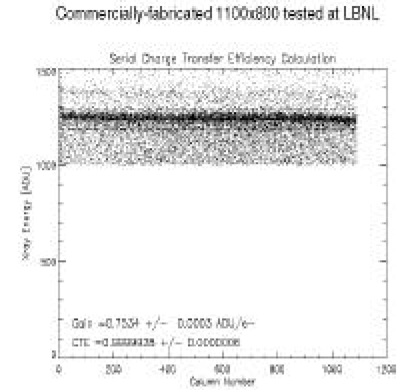
Non-optical Measurements

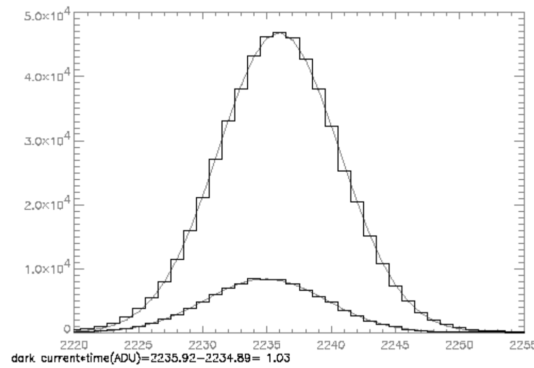
Read noise

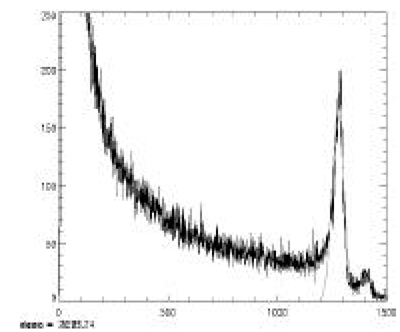
Dark current

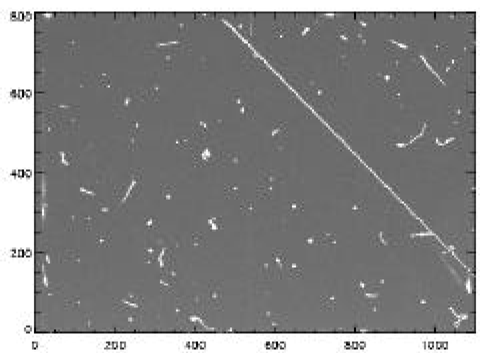
Charge Transfer Efficiency

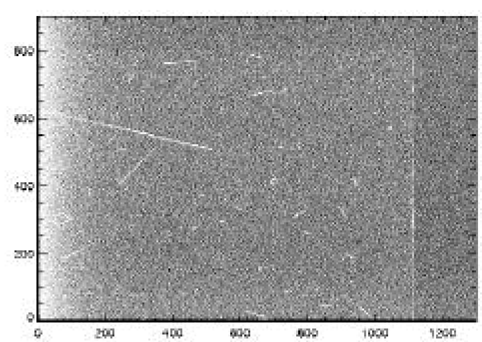


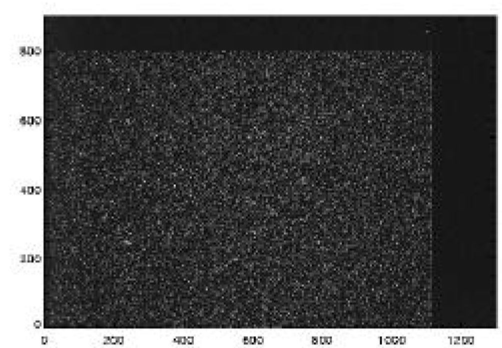








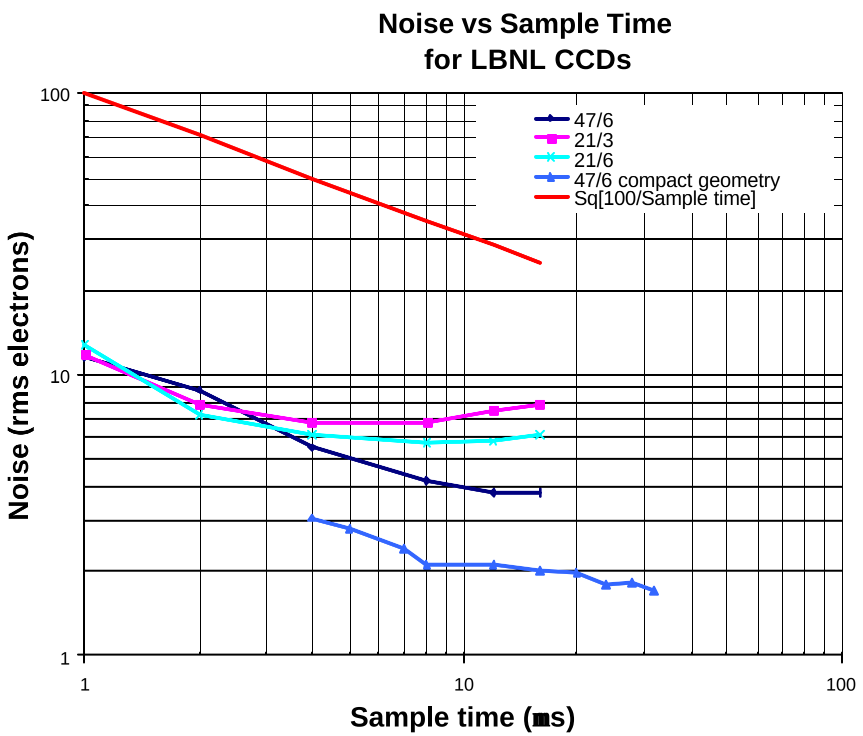


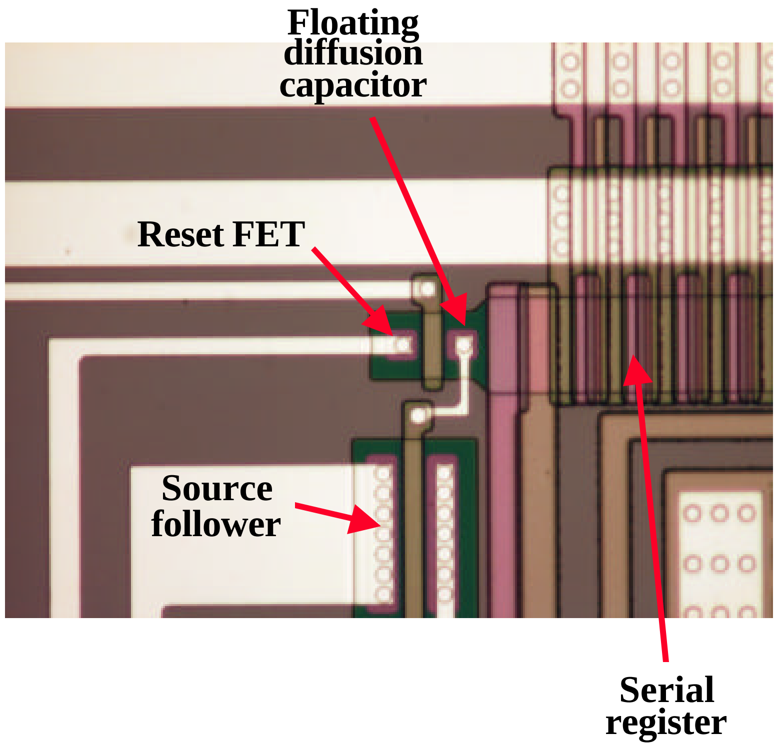


Read Noise Measurements

Noise after correlated double sampling.

Low capacitance readout geometry.
Read noise of 2e and sensitivity of 6 μV/e.



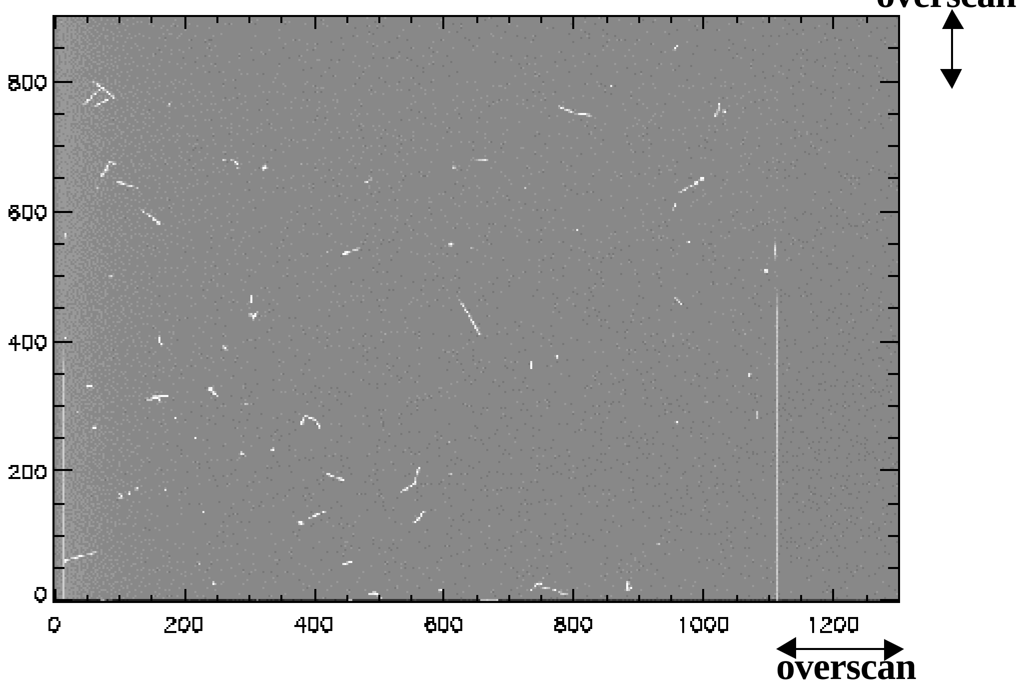


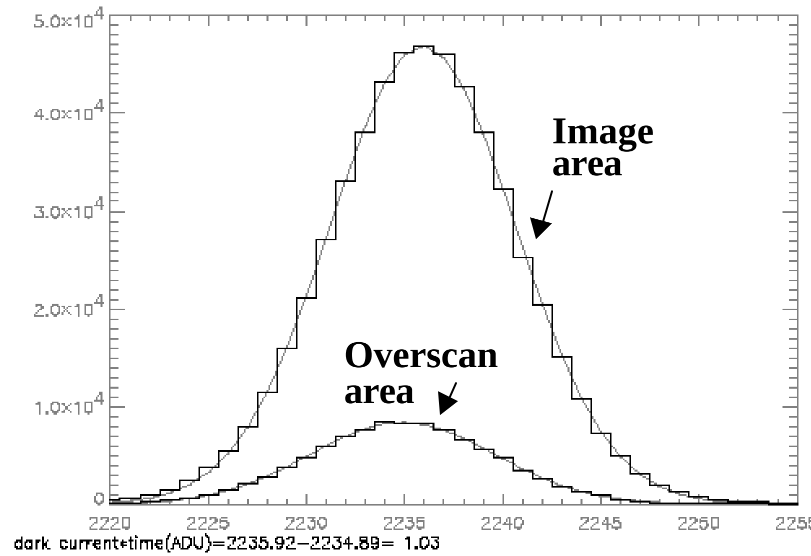
Sample time is the width of the reset or video integration.

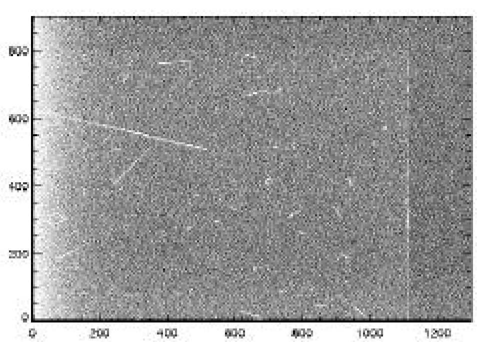
Measurements courtesy of Lick/UCSC.

Dark Current Measurement

800 x 1100 CCD







Measured dark current per 1000 sec obtained by fitting image area and overscan areas and subtracting gaussian peaks.

Dark charge collected = 1.03/(0.41*1000) = 0.0025 e-/s or 9.0 e-/pixel/hour.

CTE Measurement

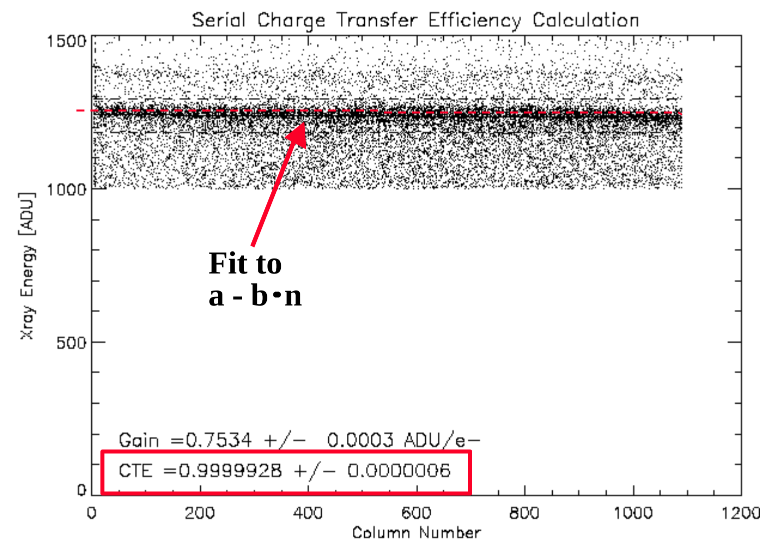
For every pixel to pixel charge transfer there is the potential for some charge loss.
CTI is the charge transfer inefficiency.
People often quote the more awkward complement, the charge transfer efficiency.

A CTI or CTE is quoted for both the serial and parallel transfers.

We use the Mn k**a** x-ray line of 55Fe as a known deposition of 1620 electrons.
We see how well 1620 electrons is reconstructed as a function of position in the CCD.
CTI of 5 x10^{-6} are typical.

note

Commercially-fabricated 1100x800 tested at LBNL

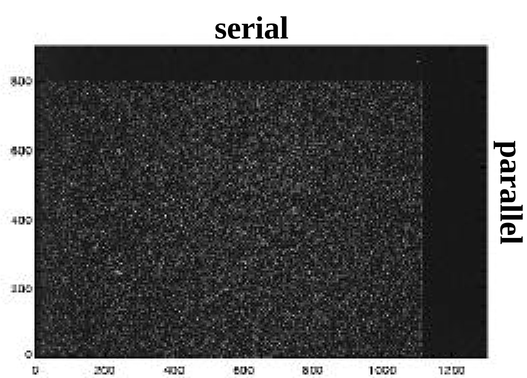


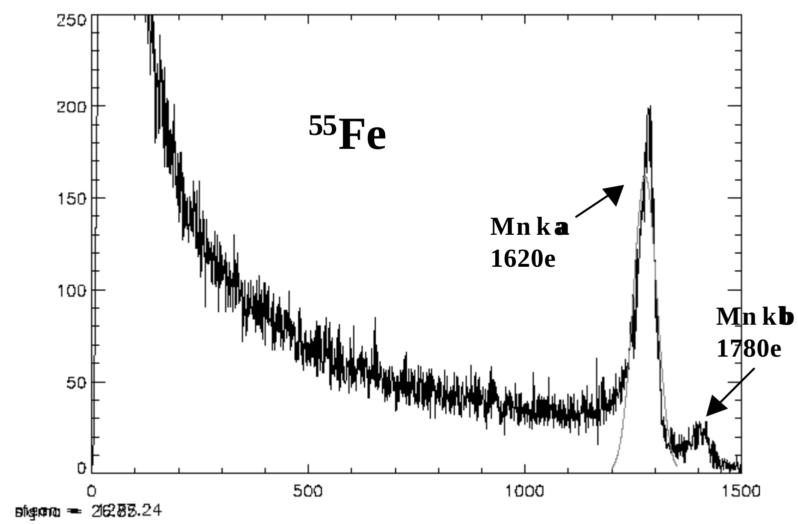
$CTI = 1 - CTE$

$CTI^n = (Q_1 - Q_n)/n = b*n/a$

$CTI = b/a$ for $b/a<<1$

(n is the number of rows or columns)

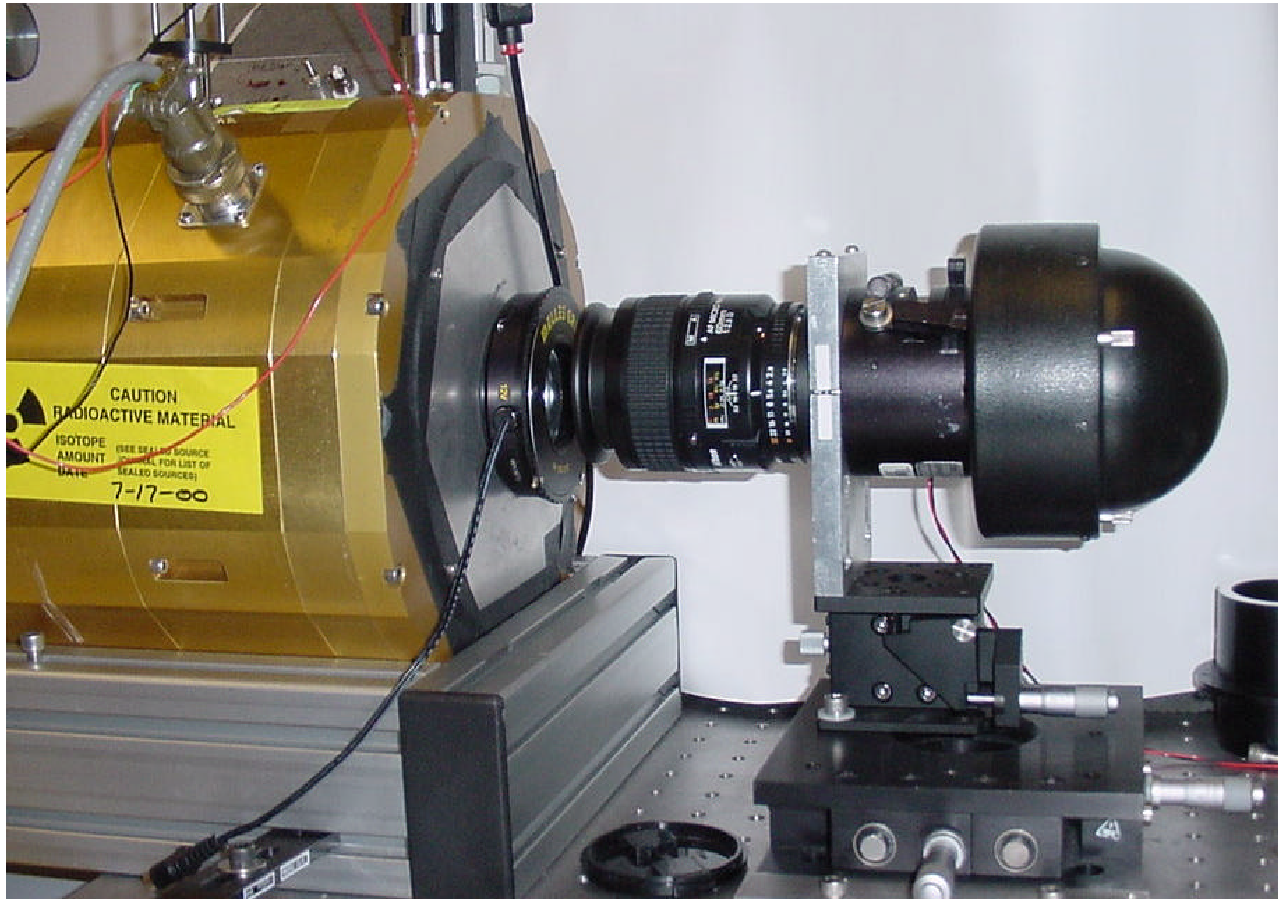




Optical Measurements

Present abilities
- Linearity
- Well depth
- Erasure

Need to develop
- CTE *vs* charge
- QE
- MTF
- Trap density
- Cross talk



View showing dewar with attached shutter and Optoliner projector fitted with Nikon macro lens and xyz stage.

Linearity and Well Depth

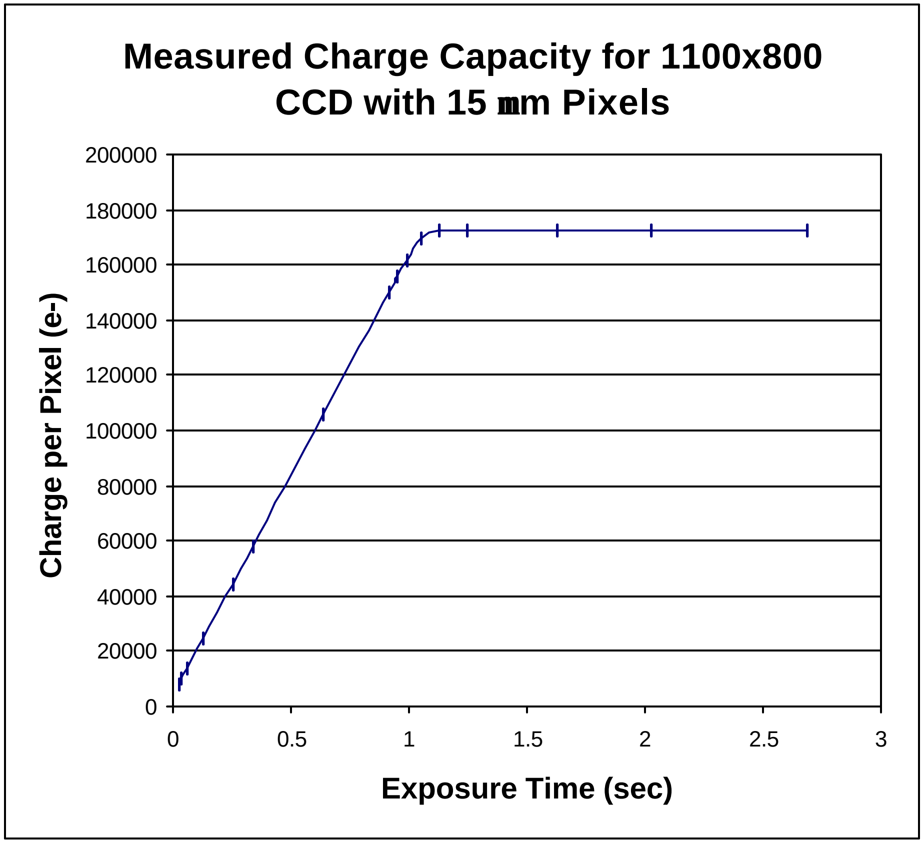
Well depth is a function of pixel size.

We are interested in small pixel sizes for SNAP to minimize area.

We have 10.5, 12, and 15 μm pixel sizes to test.

Scaling law is not obvious and needs to be measured.

Preliminary 12 μm well depth found to be 150 ke.



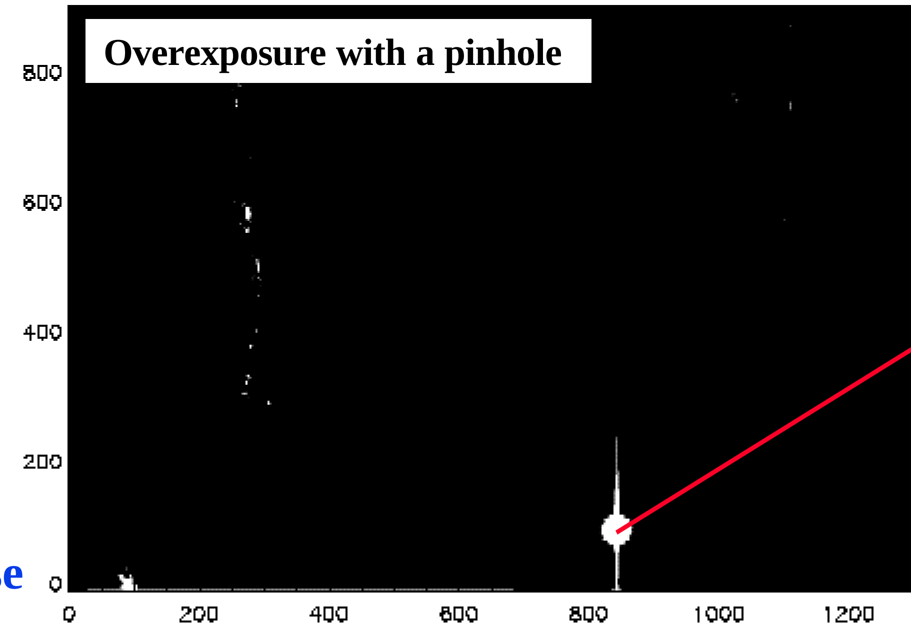
- Saturation curve obtained by plotting peak projected spot intensity versus exposure time.
- Full-well capacity in electrons obtained by scaling ADU's by CCD gain.

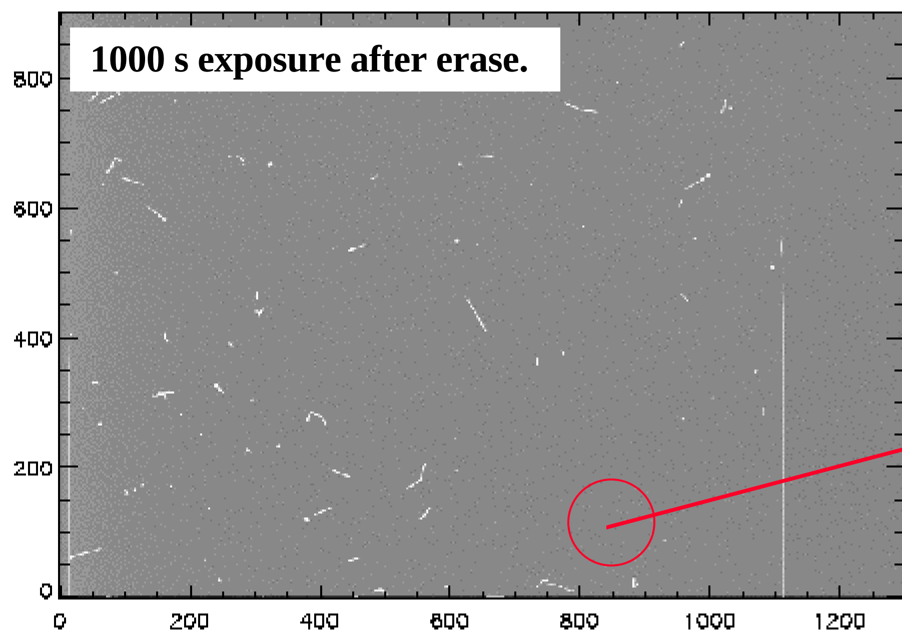
Persistent Images

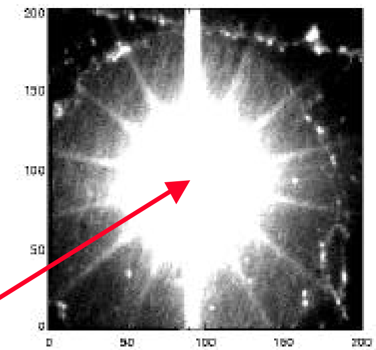
Saturated images can persist for hours.

We have an effective erasing technique — flood channels with electrons.

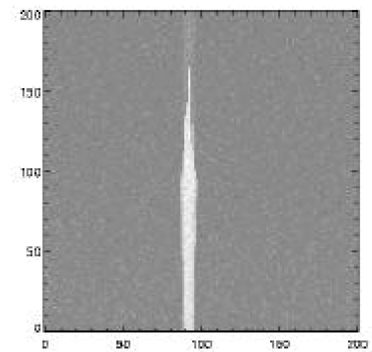
Observe lowest dark currents after an erase cycle.



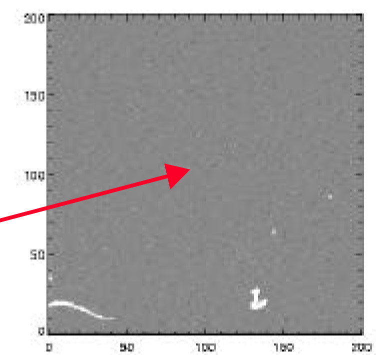




Saturating exposure



Persistent image



Erased image

Radiation Tolerance

Radiation testing done at LBNL 88” Cyclotron with 12 MeV protons.
(Scaling other results at different energies is straight forward.)

We measure FET I-V and sub-threshold curves (300 K), dark current, read noise, and serial and parallel CTE pre- and post-radiation (150 K).

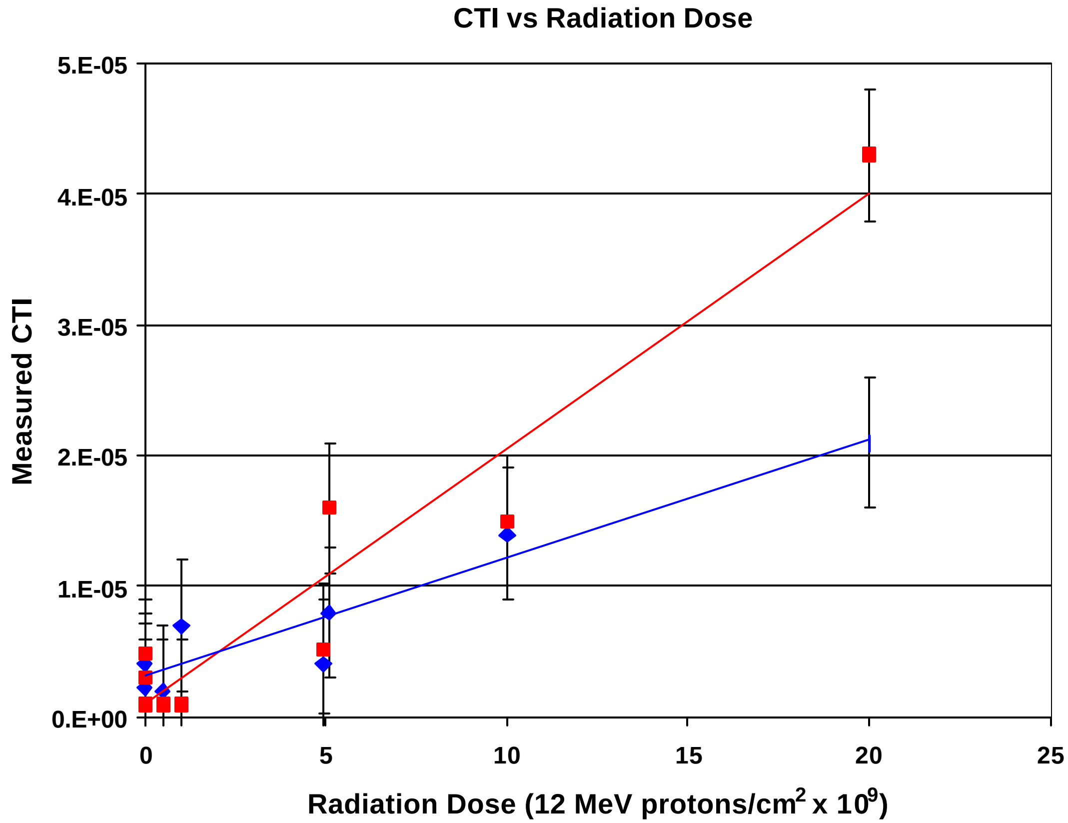
The will be an ongoing activity for the next two years – large phase space to map out.

Tested devices (all 15 μm)

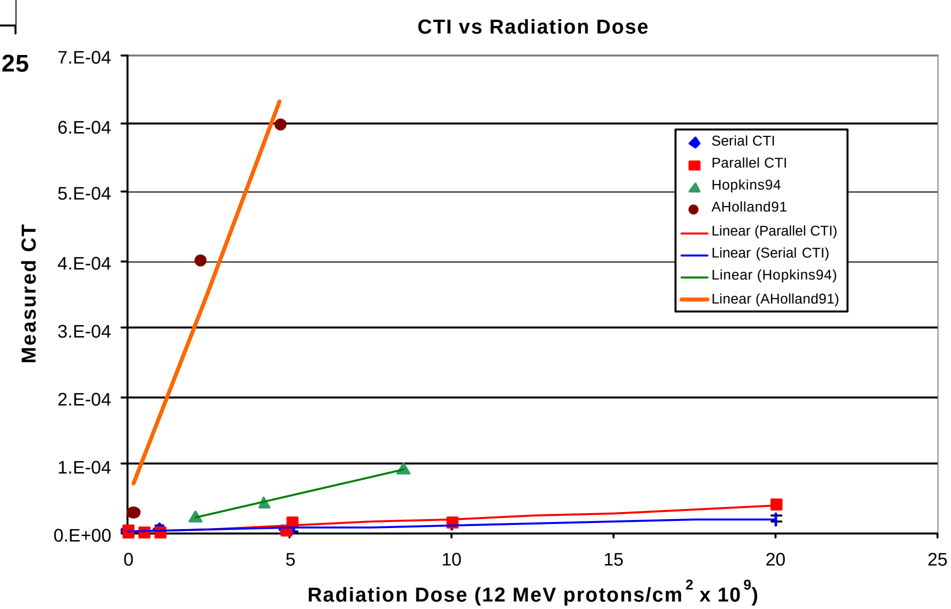
CCD	Type		Radiation Dose (protons/cm^2)	
		1st Pass Total	2nd Pass Total	3rd Pass Total
W4U	1100 x 800	5.0×10^{8}	5.0×10^{9}	
W2U	1100 x 800	1.0×10^{9}	1.0×10^{10}	
W2L	1100 x 800	5.0×10^{9}	2.0×10^{10}	

Devices were exposed at room temperature and unpowered.

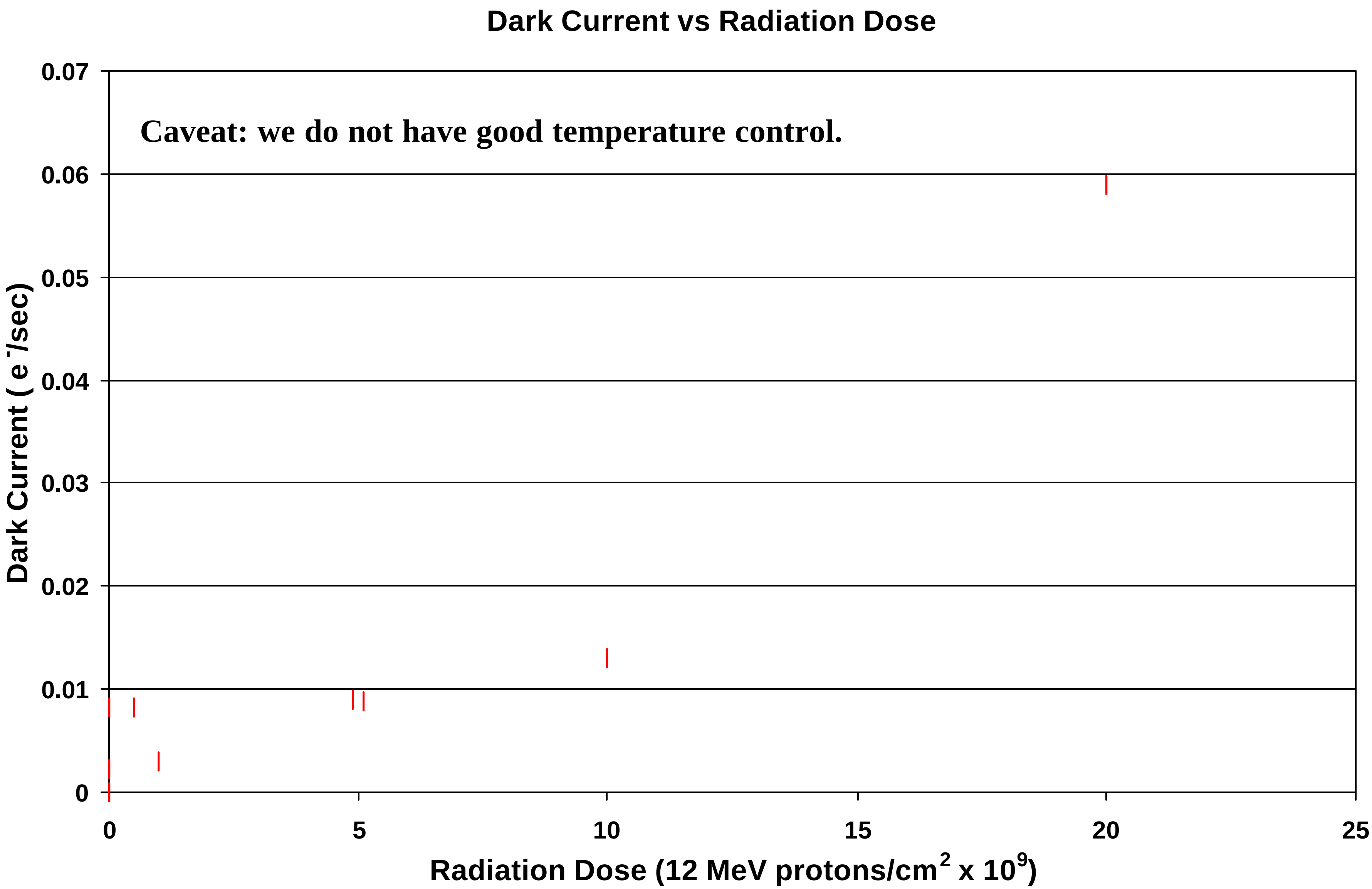
Radiation Tolerance cont.



An estimated NIEL dose for 3 years during solar max is 2 x 10^7 MeV/g.
This is equivalent to 10^9 12 MeV protons.



Radiation Tolerance cont.



Radiation Tolerance cont.

- Near future plans:

  —After making some scheduled improvements in the test instrumentation (system noise reduction, better temperature regulation), we plan to incrementally increase the proton dose levels on the above CCD's to obtain additional damage data.

  — Irradiate Commercialized CCD's for comparison.

  —Developing new test protocols designed to produce additional damage information, *e.g.*, pocket pumping to monitor trap development.

- CCD improvements

  —We note that the serial register already has an additional notch implant in the channel for enhanced small charge CTE and radiation tolerance.

  —In the 12 μm device we are submitting, the parallel channels will also have a notch implant.

Diffusion

Diffusion

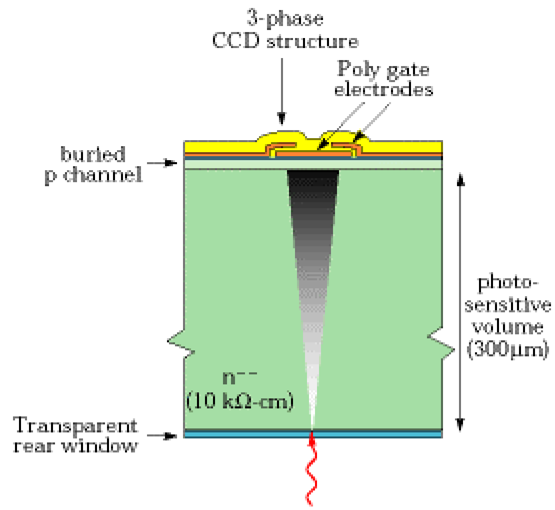
Issue

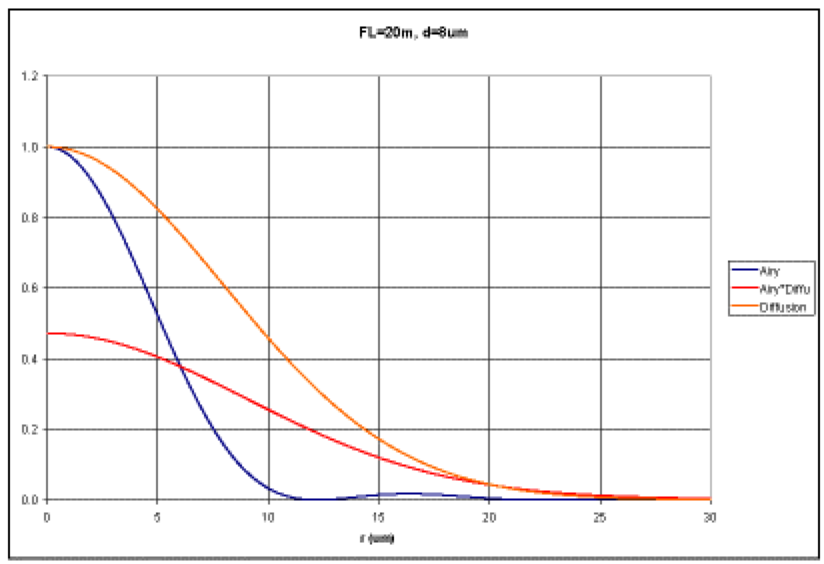
Diffussion scale for 300µm thick CCD is 7µm at 60V depletion.

This is comparable with the Airy disk width for D=2m, FL=20m: 5µm at 10000A.

Can dilute the impact linearly by increasing the FL.

Can dilute the impact by $V^{-1/2}$ and/or thickness[1].





Diffusion cont.

Diffusion

Scaling law

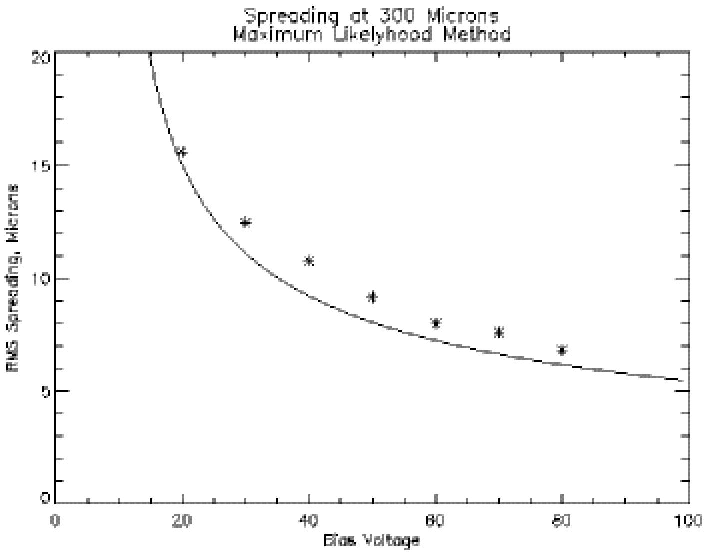
$D = (2 \cdot k \cdot T/q) \cdot \mu_p = 13mV \cdot \mu_p$ at 150K

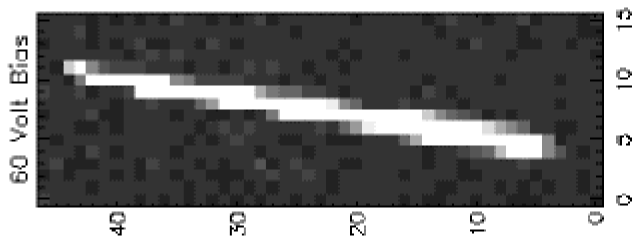
$\sigma = \mathrm{Sqrt}(2 \cdot D \cdot t)$

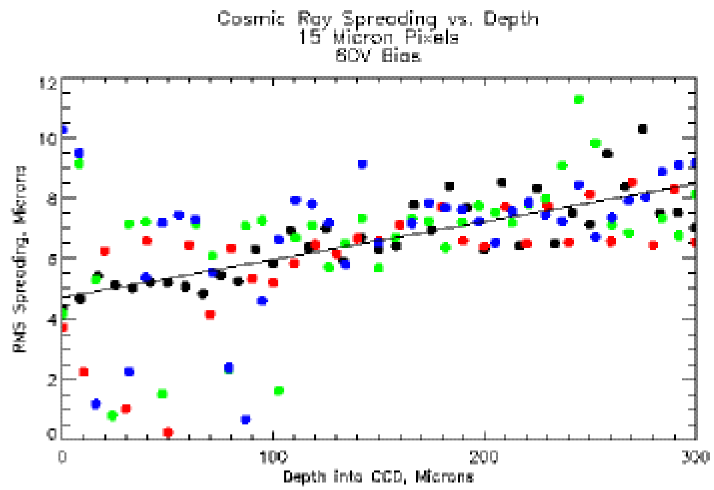
$t = d/v_{drift}$ where d is the thickness

$v_{drift} = \mu \cdot E$

$\sigma = \mathrm{Sqrt}(0.026 \cdot d/E) = \mathrm{Sqrt}(0.026 \cdot d^2/V)$



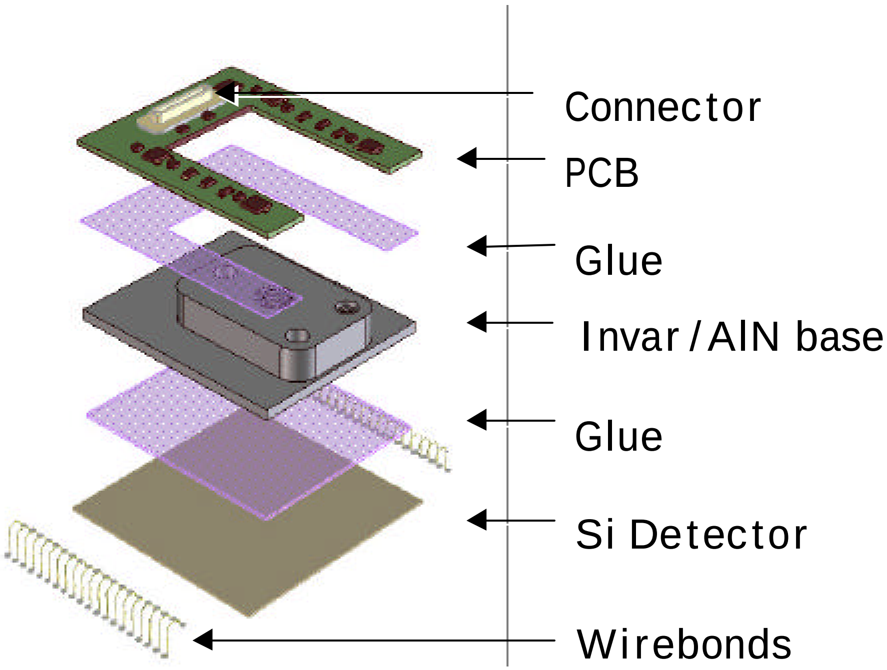


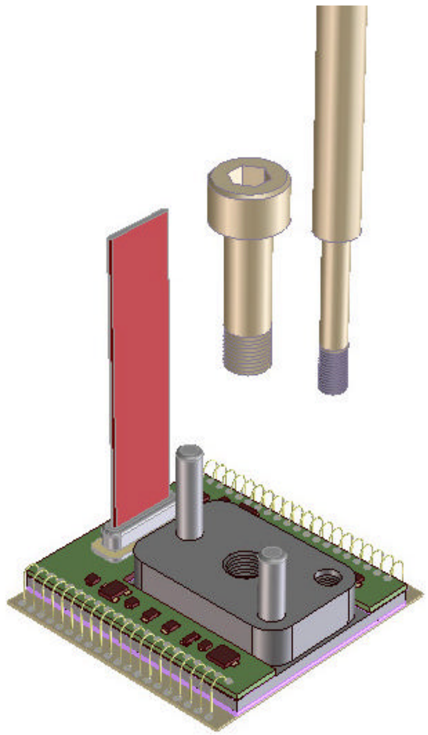


CCD Packaging

Packaging

- Support CCD
- Connection to cold plate
- Four-side abuttabe for dense mosaic.
- Build-in mechanical precision – no shimming.
- Access to bonding pads
- Local electronics
- Cable connector
- Low background radiation materials





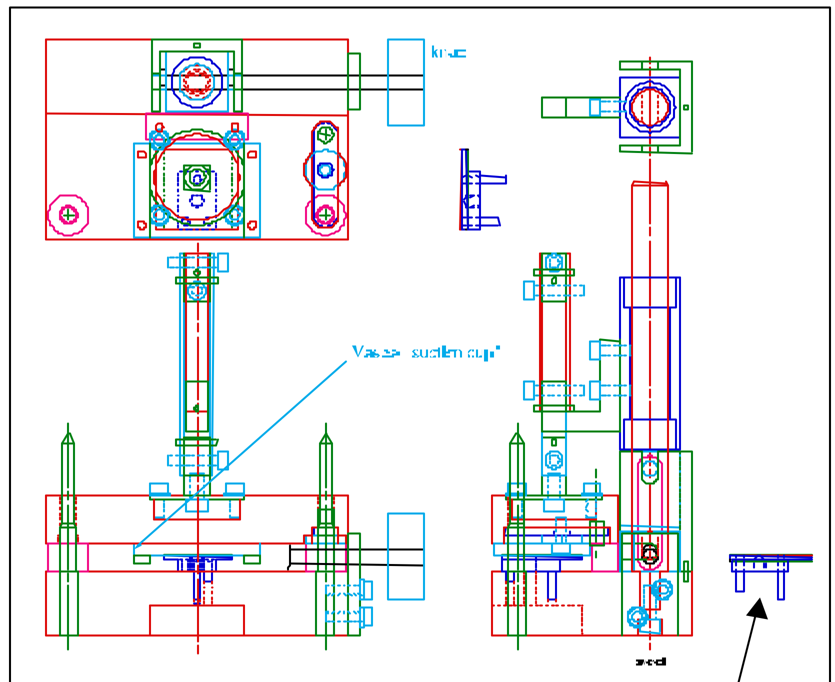
CCD Assembly

Class 10000 cleanroom

- Laminar flow bench
- Wire-bonder

Alignment and gluing assembly fixture

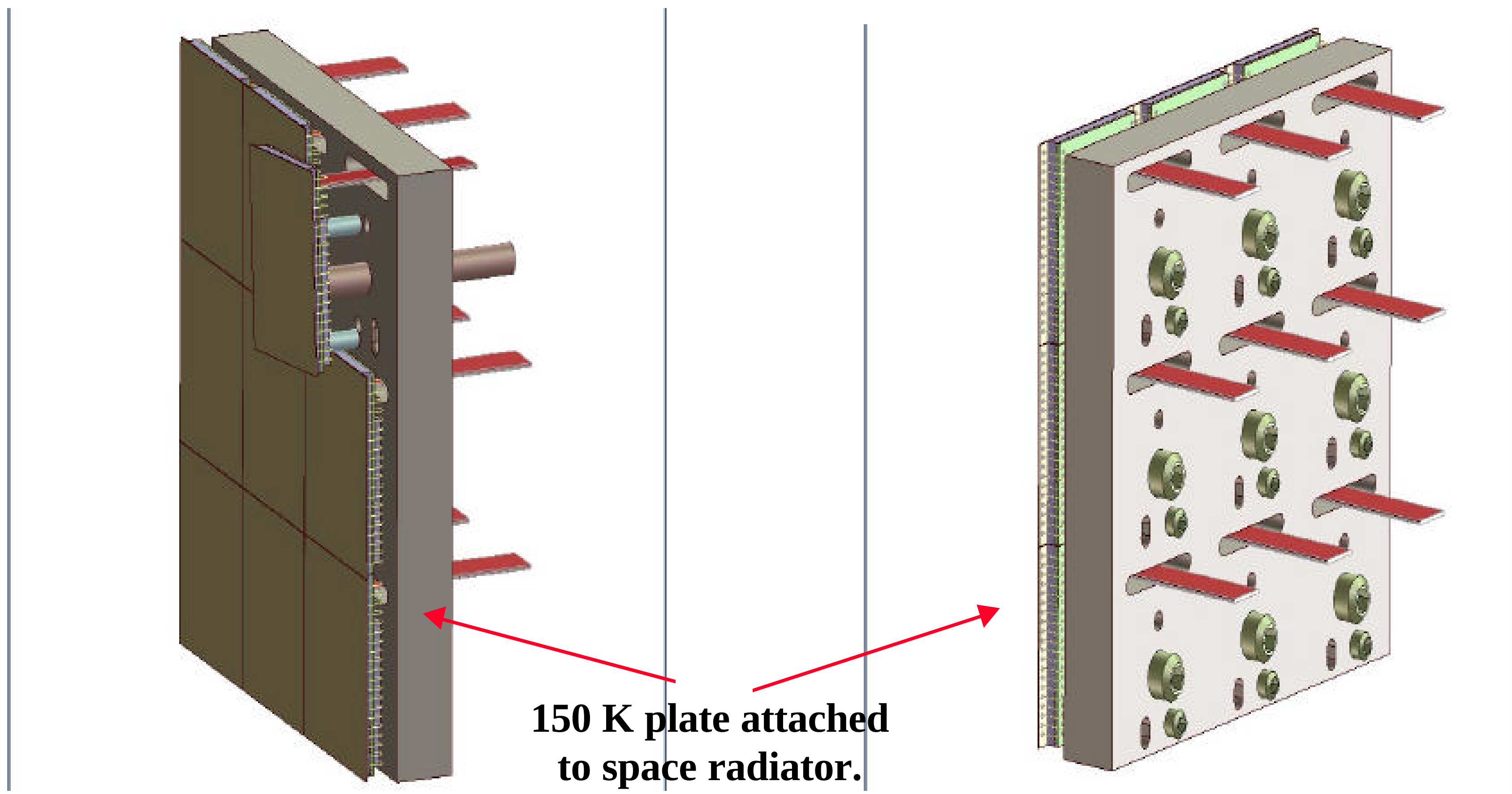
- Works for devices as large as 2k x 4k, 15 mm.
- Vacuum chuck can go into 150 C oven, if req'd.
- Vacuum chuck fits under wire-bonder head.



CCD module

Mosaic Packaging

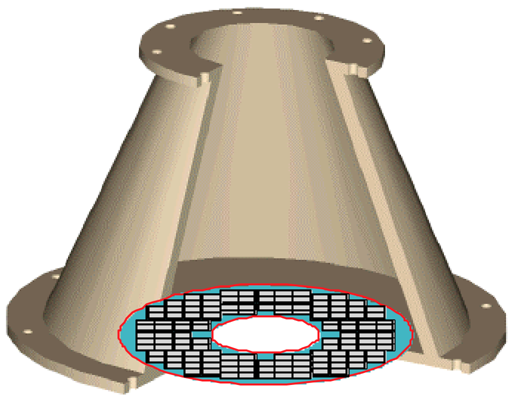
With precision CCD modules, precision baseplate, and adequate clearances designed in, the focal plane assemble is “plug and play.” Final assembly can be surveyed cold.



Shielding

Develop a CCD focal plane shield concept to reduce:

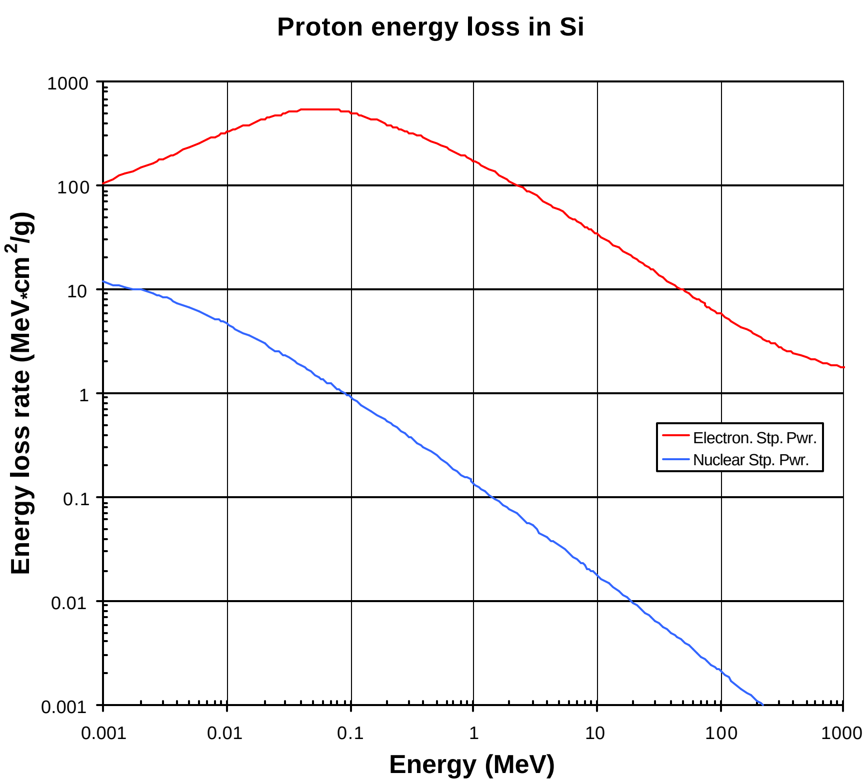
- **Stray light.**
- **Particle backgrounds — calculate doses on imager; do electronics exposure at the same time.**
- **Black body thermal loads.**

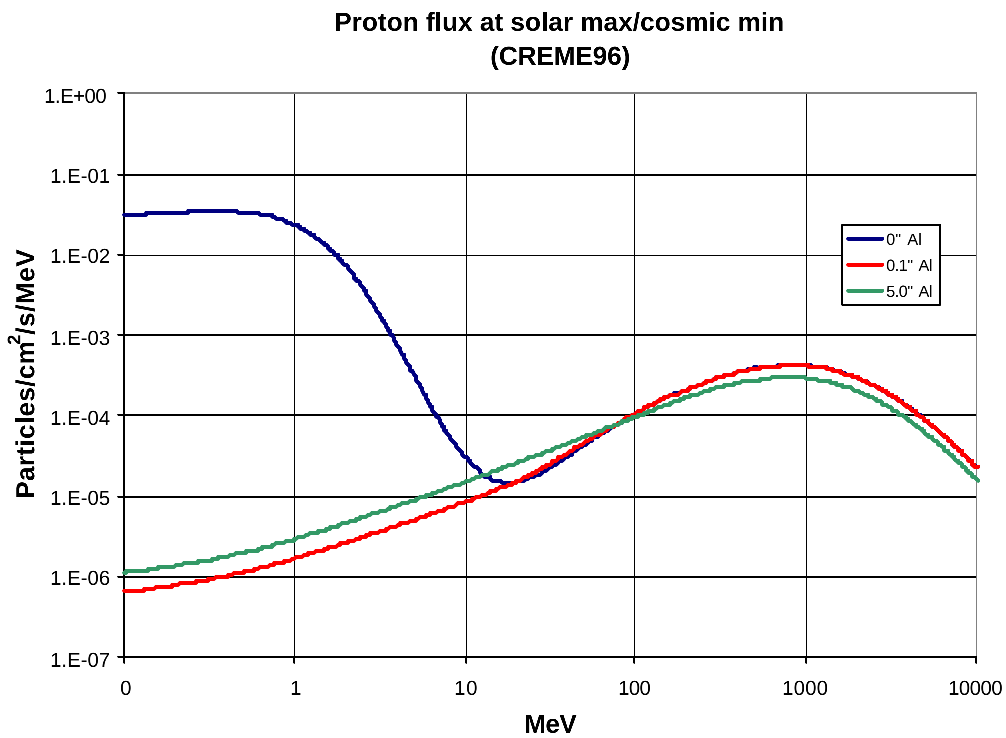


Particle Shielding

Particle background has two components
•Solar protons — sub-100 MeV
•Galactic cosmics

Solar protons are most damaging to CCDs and some shielding makes a big impact.





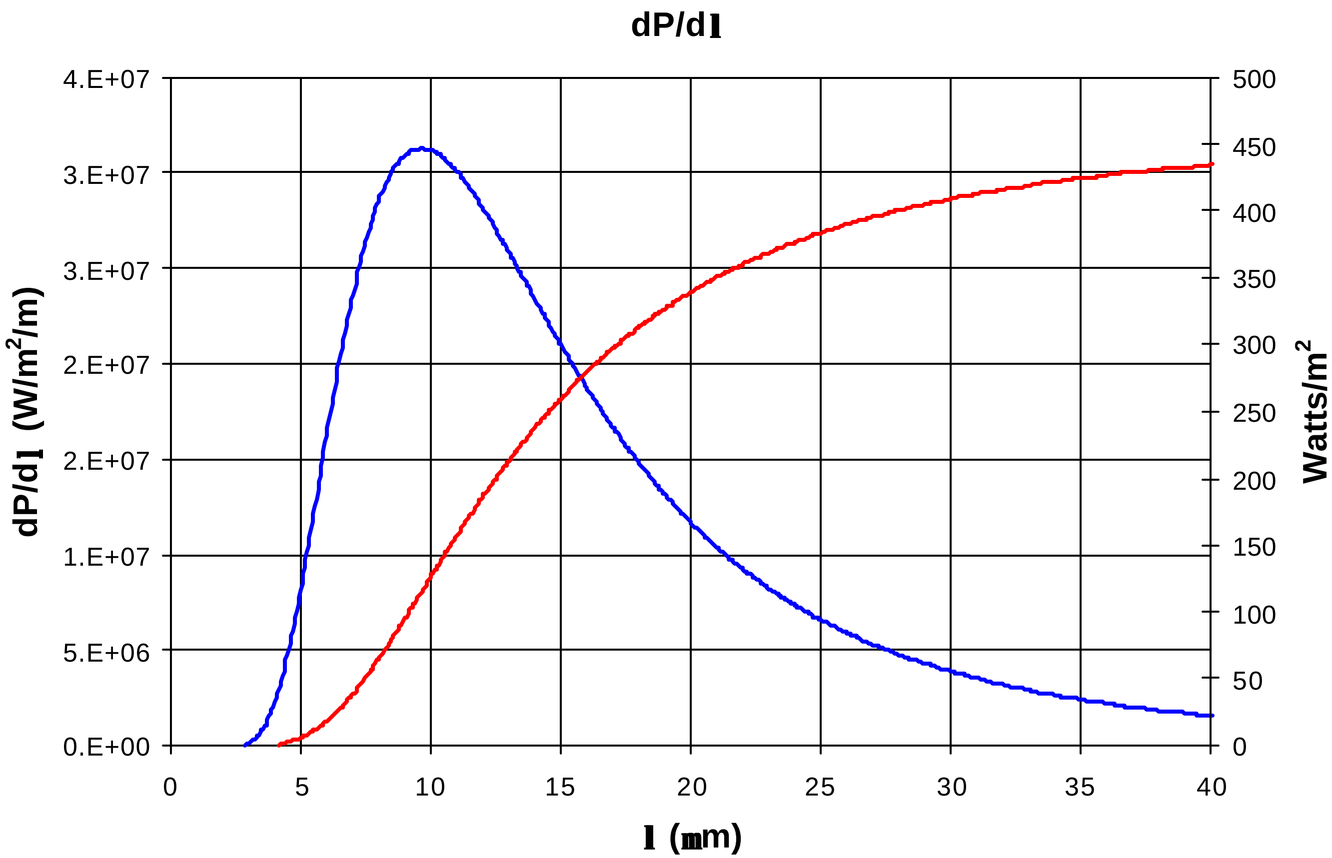
Design a shield by minimizing the convolution of flux, material attenuation, and energy loss in silicon.

Thermal Shielding

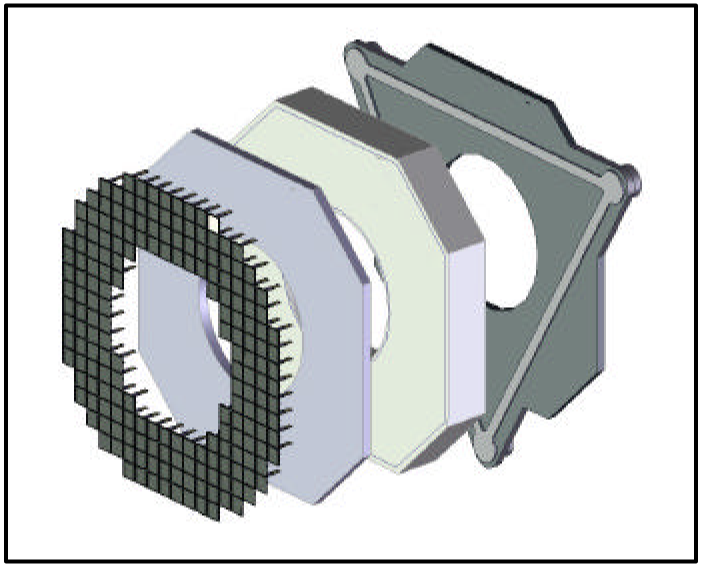
Black body at 300 K is a thermal load, not an optical load, ~450 W/m^2.

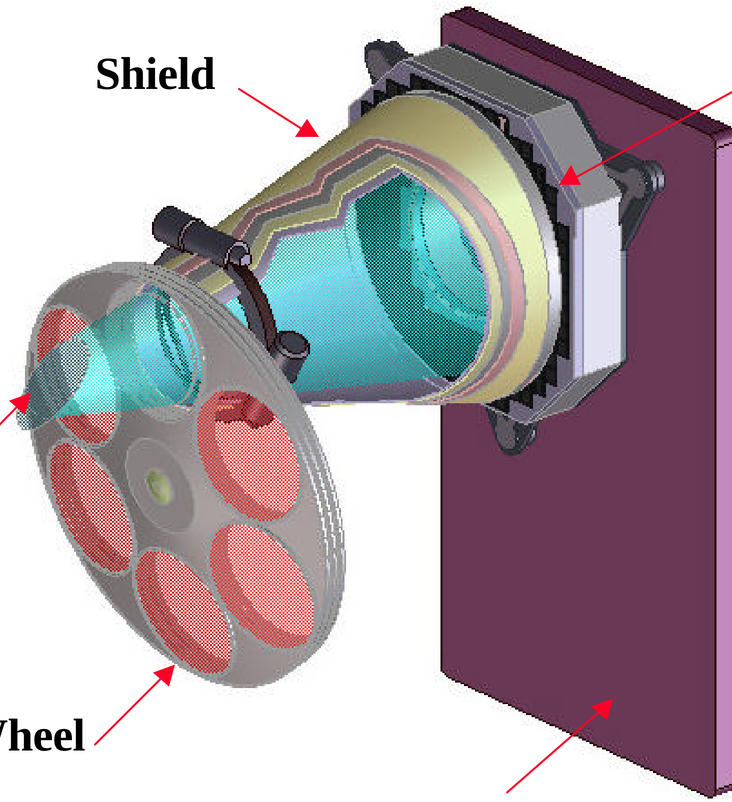
GigaCam is ~0.1 m^2, $\Rightarrow$ ~50 W if nothing done.

Use the particle shield as a thermal baffle to reduce solid angle.

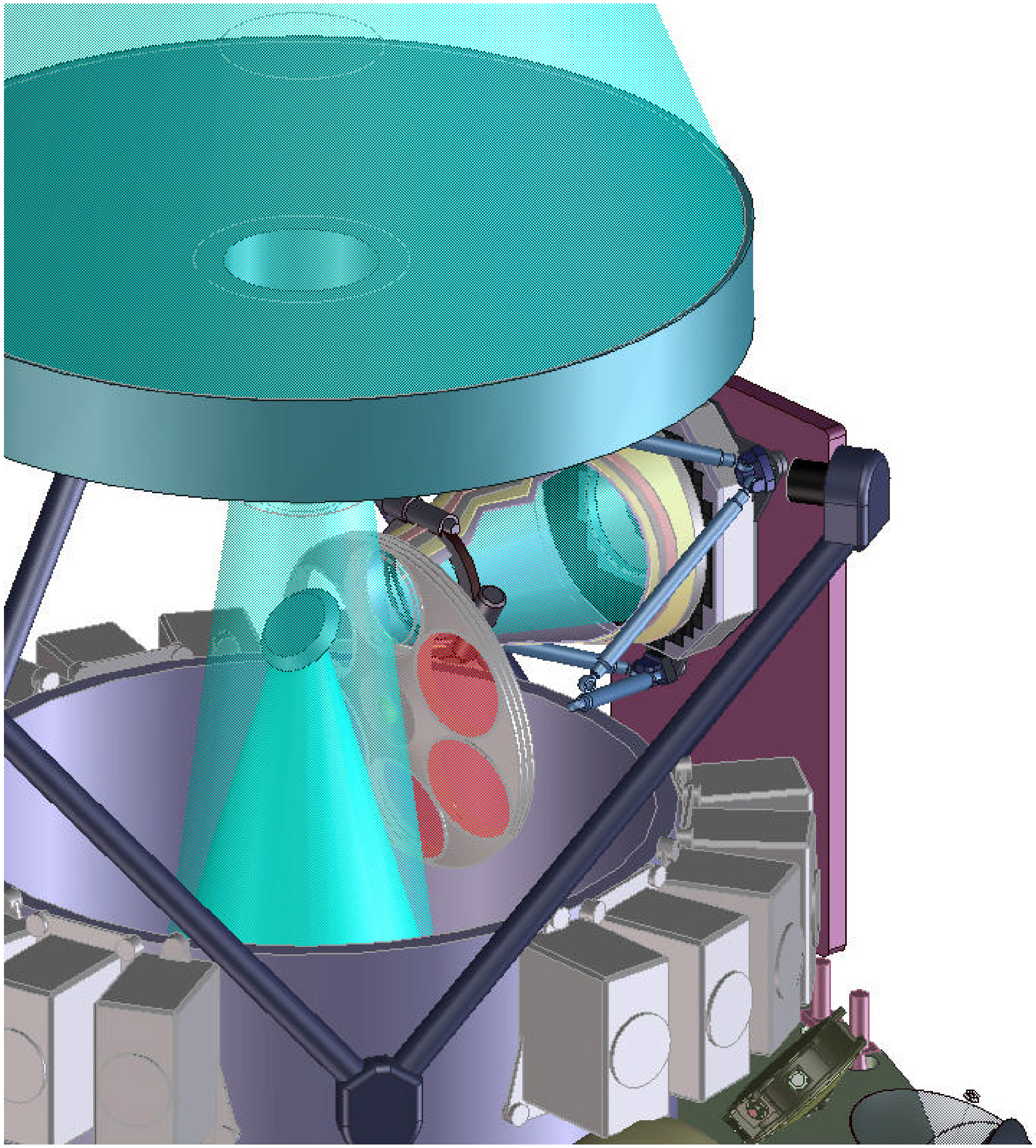


GigaCam Assembly





GigaCam Mounted in SNAP



Summary

The high resistivity, *n*-type, *p*-channel, fully depleted silicon technology has produced functioning CCDs with good noise and QE performance.

Early evidence is that the technology is sufficiently radiation tolerant for the SNAP mission.

The commercial foundry has made successful parts.
We will exercise this foundry several times over the next 18 months.
SNAP-like parts will be available in April.
300 μm thick, AR coated parts available in June.

We have built a team to test CCDs.
We will be expanding our test capabilities to do more types of optical measurements.
The next 18 months will see a lot of detailed measurements to fully understand the device characteristics.

From the above activities, we will have a good grasp on the time and effort and associated costs to produce CCDs for GigaCam.